WVGA041S Series
Low-Power AMOLED Microdisplay

Data Sheet

Pre-Spec V0.1

WVGA041SCV1

WVGA041SWV1

WVGA041SGV1

For Products:

WVGA041SCV1	—	Full Color
WVGA041SWV1	—	Monochrome White
WVGA041SGV1	—	Monochrome Green

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1 FEATURES

1.1 Description

- Si-Base AMOLED Microdisplay
  - 0.18μm CMOS Technology
  - Full Digital Video Core
  - High Efficiency Top Emission Structure
  - Low Power Consumption
- Up to 800×480 (WVGA) Resolution
  - View Area: 0.41 inch
  - Pixel Pitch : 11.1μm
  - Total Pixels : 804 (×3)× 484
- Digital Video Interface
  - Compatible with ITU-R BT.656/601
  - Accept 8/16/24-Bit Digital Video
  - Accept YCbCr/RGB Color or Mono
- Wide operating temperature (-40℃~+65℃)
- Digital Video Signal Enhancement
  - Brightness
  - Contrast
- Gamma Correction
  - 10Bit 256Level RGB Separated Gamma LUT
  - 14 points Linear Gamma
- Full Scale 10-Bit DAC
- Support Binocular Stereovision
- Horizontal/Vertical Mirror
- Shift and Position Control
- Embed Temperature Sensor
- Integrate 9-Bit ProgrammableVcom Module
- Built-in Test Patterns
- IIC Interface \ 3-Wire SPI Interface

1.2 Products Coding

WVGA 041 S C V1 R1

① ② ③ ④ ⑤ ⑥

①Type	
WVGA	800×480
SVGA	800×600

③ Temperature	
S	Standard : -40℃～+60℃
N	Normal : -10℃～+40℃

⑤Connector	
V1	Board to Board
V2	FPC

②Size	
041	0.41 Inch
050	0.50 Inch
060	0.60 Inch

④Color	
C	Full Color
W	Mono White
G	Mono Green

⑥Revision	
R1	Revision No.

2 INTRODUCTION

WVGA041S series AMOLED microdisplay fabricated by OLiGHTEK's proprietary top emitting and high luminance efficiency Si-Base AMOLED technology. WVGA041S series microdisplay includes full color, Monochrome white, Monochrome green and other specifications. With the same interface and pin definition, WVGA041S series products have 8.9244mm×5.3724mm (0.41 inch) display area, and supported less than or equal to WVGA resolutions format.

With proper optic enhancement devices, the microdisplay can provide high quality, large virtual image.

WVGA041S series microdisplay's silicon substrate is fabricated by 0.18μm CMOS technology, integrated full digital video signal processing, 804×484×3 active driving units, digital logic control, scan distribution, D/A converting, temperature sensor, gamma correction, DC-DC for cathode's negative voltage, two-wire serial communication interface and so on. The input video signal is compatible with ITU-R BT. 656/601 and support 8/16/24 bits digital video. The function of microdisplay such as display mode, scanning direction, display position, brightness, contrast and gamma correction can be programmed through the two-wire serial communication interface. The digital interface voltage level is compatible with 1.8~3.3V CMOS standard. The microdisplay operate on 5V&1.8V power supply and can be applied in various near-to-eye display systems that demand compact size, high resolution, low power consumption and wide working temperature range.

2.1 Characteristic Parameters

Model		**WVGA041S**		
Product Type		**Color**	**Monochrome White**	**Monochrome Green**
Resolution		800 (×3) × 480		
Active pixels		804 (×3) × 484		
Pixel Aspect Ratio		1:1		
Color Pixel Arrangement		RGB Vertical Stripe		
Gray Levels		8bits/256Levels		
Gamma Correction LUT		3×256×10Bit		
Luminance Uniformity		> 90%		
Contrast		> 10000:1		
Digital Video Interface		ITU-R BT.601/656 24-bit，4:4:4，RGB/YCbCr 16-bit，4:2:2，YCbCr 8-bit，4:2:2，YCbCr/Mono		
Operating Temperature		-40℃ ～ +65℃		
Chromaticity	**White**	CIEx=0.30±0.05, CIEy=0.35±0.05		
	Green			
Operating Humidity		≤85%RH (Non condensing)		
Pixel Size(μm²)		11.1 × 11.1		
Viewing Area(mm²)		8.9244 × 5.3724		
Mechanical Envelope(mm³)		22 × 17 × 5.2		
Operating Luminance(Cd/m²)		>70	>100	
Power Consumption(mW)		<200	<200	
Lifetime(Hours)		25000	25000	
Power Supply	**DC 1.8V(mA)**	⩽50		
	DC 5.0V(mA)	⩽200		
Weight(g)		⩽1.8g		

2.2 Product Structure

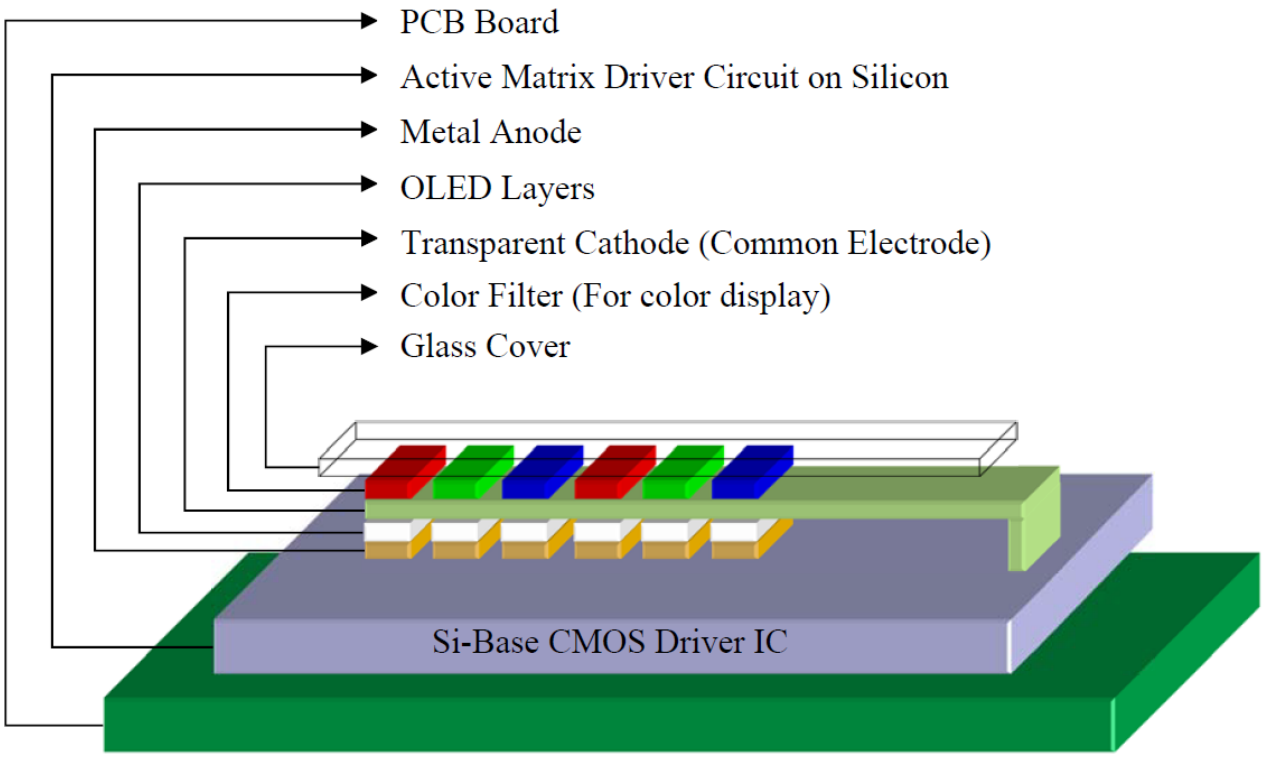


Figure 2-1 WVGA041S series device's structure

OLiGHTEK's WVGA041S series AMOLED microdisplay is manufactured on a silicon substrate which is integrated with video signal processing and active driver, then followed by sub-pixel metal anode, multi-layer OLED light-emitting film, transparent cathode(common cathode), compound high density sealing film, RGB color filter layer, etc., after which paste glass cover to protect the microdisplay, and bond with PCB board. Figure 2-1 shows the device's structure.

2.3 Pixel Array

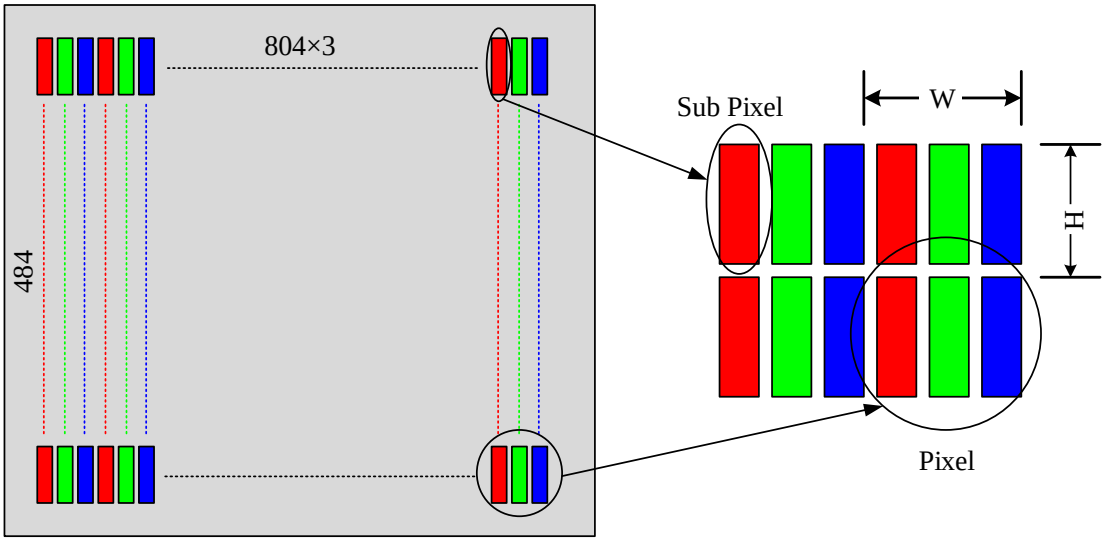


Figure 2-2 Pixel and Sub-Pixel Array

Each pixel of OLiGHTEK's WVGA041S series AMOLED microdisplay is formed by three sub-pixels (Figure 2-2). The pixel's related parameters are shown below:

Model	Pixel Size		Duty Cycle	View Area	
	Width(W)	Height(H)		Width（804×W）	Height（484×H）
WVGA041S	11.1μm	11.1μm	69.5%	8.9244mm	5.3724mm

Each sub-pixel of colorful display emits white light, and full-color display is fulfilled through the RGB color filter. Since there is no color filter, the luminous efficiency of the monochrome display is higher than the color display.

2.4 Function Diagram

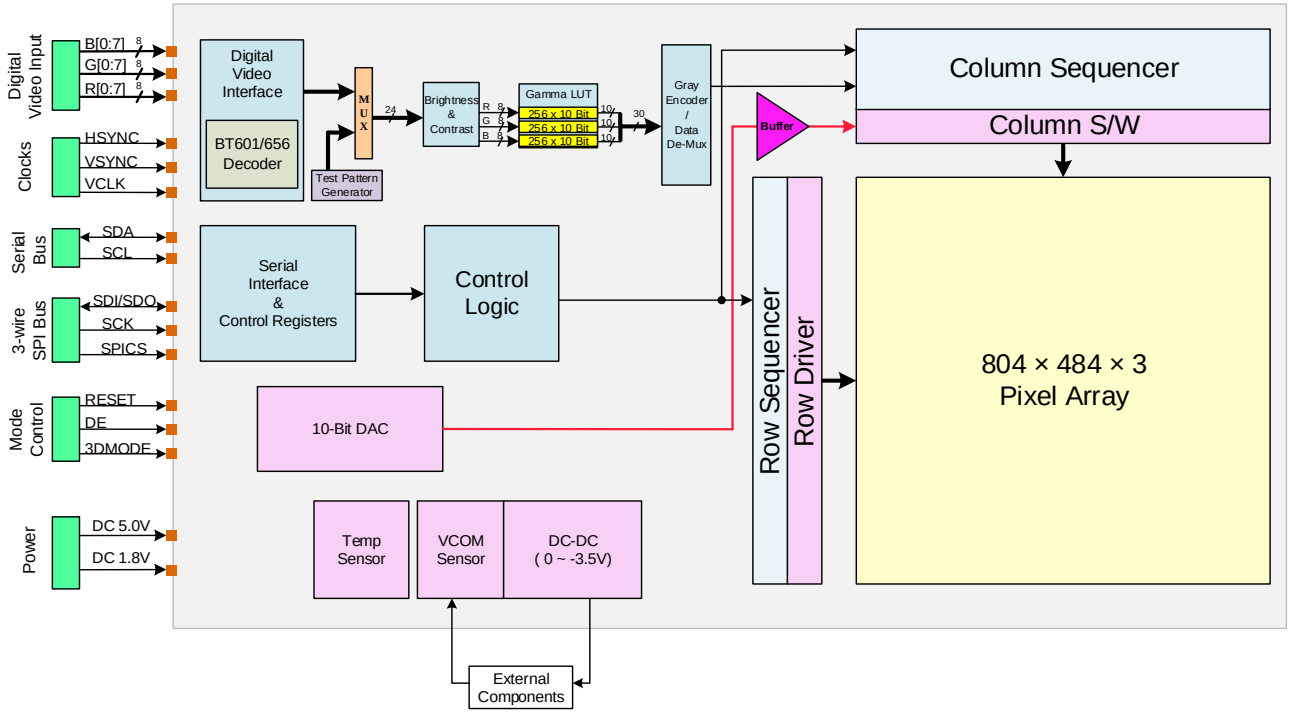


Figure 2-3 WVGA041S Series Architecture & Principle Diagram

Figure 2-3 shows top level block diagram of WVGA041S series microdisplay's driver circuit. The chip is mainly composed of the digital video signal interface and decoder, digital video signal processing, digital Gamma correction, gray mapping, D/A conversion, row & column scanning, pixel driver array, 2-wire serial&3-wire SPI communication interface, programmable control logical unit, temperature sensor, DC/DC converter and other function modules.

Compatible with ITU-R BT.656/601 standards, digital video signal interface has three 8-bit data channels and accepts 8/16/24 bits RGB or YCbCr video signals. According to the different input formats, the internal video decoder outputs 24 bits RGB signal always. The digital video signal processing circuit receives the 24 bits RGB signal, and then adjusts the brightness, contrast respectively. The output signal is still 24 bits format and sent to the gamma correction circuit. The gamma correction circuit makes corrections of the 24 bit RGB signal by separated RGB look-up table, and extends it to 30 bits RGB signal output. By D/A conversion, the gray mapping circuit converts the three 10 bit R/G/B signals to three R/G/B analog voltage signals. The voltage stands for the R,G,B luminance, Then, the analog signal is stored in sub-pixel driving unit; driving unit circuit applies the RGB analog voltage signal to OLED's anode and holds the voltage on for one frame/field cycle time. With external 5V power supply and external components on PCB backplane, the DC/DC module generates a negative voltage which is applied to all of the OLED sub-pixels' common cathode. Under the bias voltage between the anode and the cathode, OLED keeps emitting light in one whole frame/field cycle.

Through the internal programmable SRAM (register), control logic unit deals with the digital signal, makes the different unit circuits working in harmony with each other, and realizes the binocular 3D display.

The 2-wire serial interface&3-wire SPI interface is used to realize the read/write operation of the registers,

accordingly, make the chip circuit programmable, such as digital video signal decoding and processing, gamma correction, DC/DC conversion and so on.

The internal temperature sensor circuit updates the corresponding register's numeral value which represents the real-time internal working temperature. The numeral value is read by the external control logic unit through the two-wire serial interface. According to the luminance-temperature character, OLED's common cathode's negative voltage can be adjusted by DC/DC converter so as to get proper luminance at different temperatures.

2.5 Interface & Pin Assignment

2.5.1 Connector & Pin Assignment

WVGA041S-V1 series microdisplay use a 0.5mm pitch, 40pins connector made by Hirose, part number is DF12D(3.0)-40DP-0.5. WVGA041S keeps pin-compatibility with SVGA series.

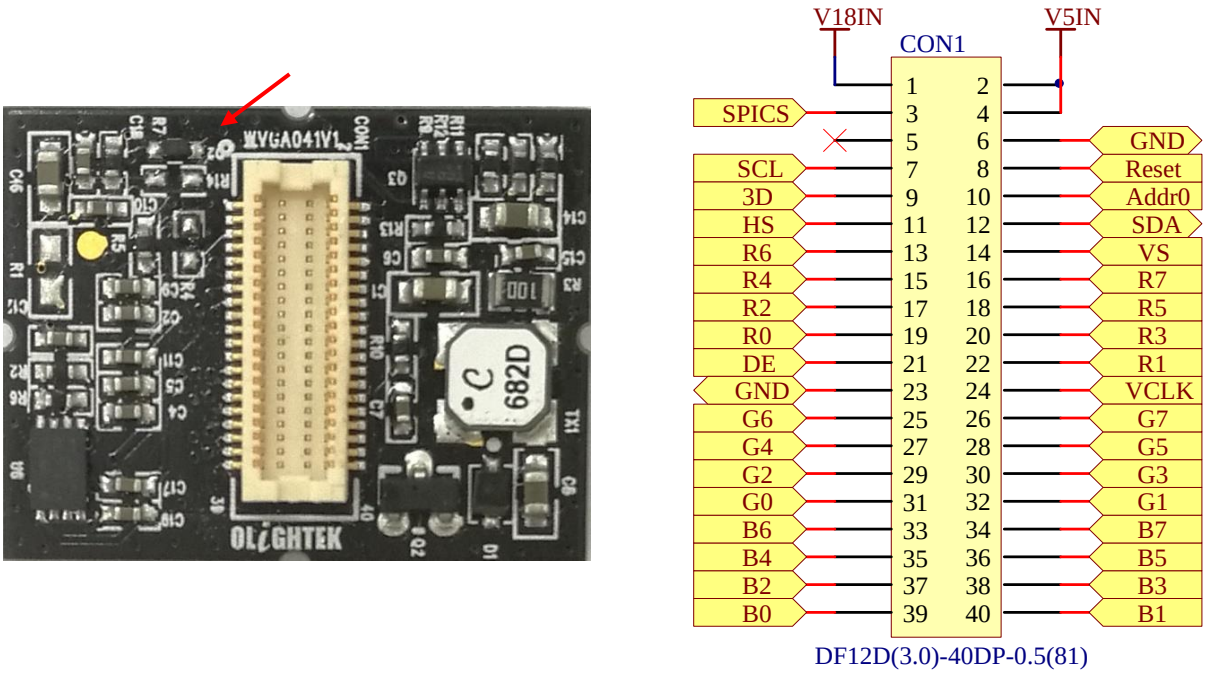


Figure 2-4 WVGA041S series microdisplay connector & pin assignment

2.5.2 Pin Definition

Table 2-1 Pin Definition

Pin	Symbol	I/O	Function	Remark	Pin	Symbol	I/O	Function	Remark
1	V18IN	P	1.8V Power Supply		2	V5IN	P	5V Power Supply	
3	SPICS	I	SPI Enable，1：IIC 0：SPI		4	V5IN	P	5V Power Supply	
5	—	—		Float	6	GND	P	Power groung	
7	SCL	I	Serial port clock line	Pull-up to 1.8V	8	RESET	I	Master reset, active low	Can not float
9	3D	I	3D L/R Signal input		10	Addr0	I	Seiral port Address A0	Pull-up to 1.8V
11	Hs	I	Hsync Signal input		12	SDA	I/O	Serial port data line	Pull-up to 1.8V
13	R6	I	Video Data Input R[6]		14	Vs	I	Hsync Signal input	
15	R4	I	Video Data Input R[4]		16	R7	I	Video Data Input R[7]_MSB	
17	R2	I	Video Data Input R[2]		18	R5	I	Video Data Input R[5]	
19	R0	I	Video Data Input R[0]_LSB		20	R3	I	Video Data Input R[3]	
21	DE	I	Data enable signal input		22	R1	I	Video Data Input R[1]	
23	GND	P	Power groung		24	VCLK	I	Pixel clock input	
25	G6	I	Video Data Input G[6]		26	G7	I	Video Data Input G[7]_MSB	
27	G4	I	Video Data Input G[4]		28	G5	I	Video Data Input G[5]	
29	G2	I	Video Data Input G[2]		30	G3	I	Video Data Input G[3]	
31	G0	I	Video Data Input G[0]_LSB		32	G1	I	Video Data Input G[1]	
33	B6	I	Video Data Input B[6]		34	B7	I	Video Data Input B[7]_MSB	
35	B4	I	Video Data Input B[4]		36	B5	I	Video Data Input B[5]	
37	B2	I	Video Data Input B[2]		38	B3	I	Video Data Input B[3]	
39	B0	I	Video Data Input B[0]_LSB		40	B1	I	Video Data Input B[1]	

2.6 Recommended Operation Ratings

SYMBOL	DESCRIPTION	MIN	TYP	MAX①	UNIT
V1.8	1.8V Power Supply	1.62	1.8	2.5	V
V5.0	5.0V Power Supply	4.5	5.0	5.5	V
$V_{I/O}$	Digital Signal Voltage②	—	1.8	3.3	V
Tstorage	Storage Temperature	-55	20	90	℃
Toperate	Operation Temperature	-40	20	65	℃

Note ①: The absolute maximum rating values (except $V_{I/O}$) of this product are not allowed to be exceeded at any time. If the product is used with its symbol value exceeding the maximum rating or in an extreme condition, the characteristics of the device maybe recovered and the lifetime of the device will decrease, even the device may be permanently destroyed.

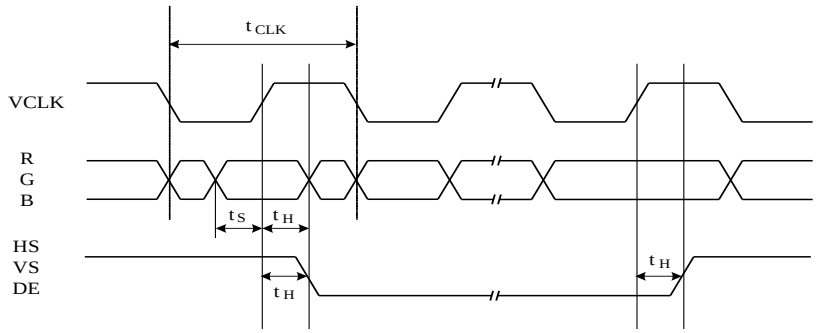
Note ②: All the Digital logic Pins (except the Power Pin) can support 1.8V/3.3V CMOS logic level.

2.7 Electrical Characteristics

2.7.1 DC Characteristics

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{1.8}$	1.8V Supply Current		9	10	12	mA
$I_{5.0}$	5.0V Supply Current		10	40	200	mA
Vcom	Cathode Voltage		-3.5	-2	0	V
Typical Power Consumption	Working	Color @ 70Cd/m2	80	120	200	mW
		Monochrome White @ 100Cd/m2	60	100	200	
		Monochrome Green @ 1500Cd/m2	-	-	-	
	Display Off		40	-	60	
	Power Down		0.4	-	2	

2.7.2 AC Characteristics



PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Digital Video Data Setup & Hold	t_S	1	-	-	ns
	t_H	1	-	-	ns
Video Clock Period	t_{CLK}	4.6	-	-	ns
Video Clock Duty	q	40	50	60	%

3 DETAILED FUNCTION DESCRIPTION

3.1 Digital Video Interface

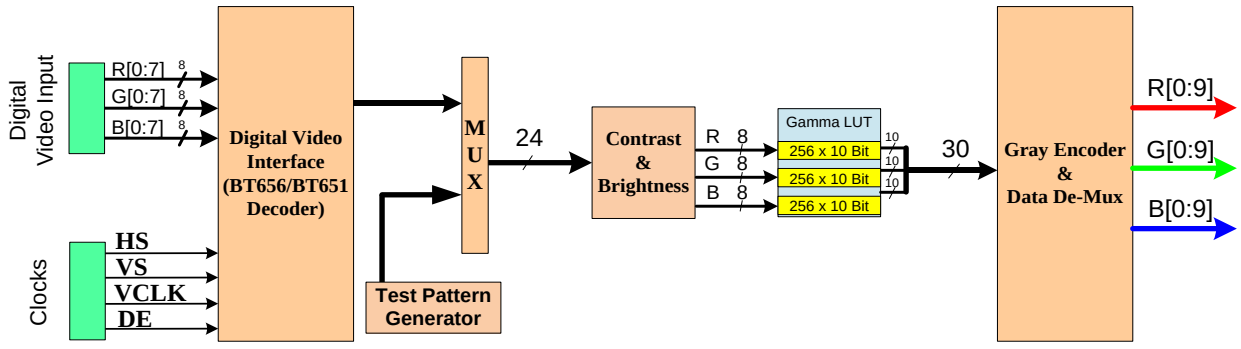


Figure 3-1 Digital Video Processing Flow Diagram

The digital video interface has three 8-bit data channels, and additional horizontal and vertical sync (HS/VS), data enable (DE), pixel clock signals (VCLK). User should select the correct signals to connect according to different

Video format. VCLK is always needed in any mode. When use 8bit with embedded sync signal (8bit ITU-R BT.656 YCbCr/Mono 4:2:2), only G[7..0] bus and VCLK are needed.

OLED Display receives data with BT601/656 format, like 8/16/24 bits and 4:2:2/4:4:4 format, and video decoder outputs 24 bits RGB signal always, then sends the signal to Video signal enhancement module and output keep 24 bits format. The gamma correction circuit makes corrections of the 24 bit RGB signal by separated RGB look-up table, and extends to 30 bits RGB signal output.

If the input video format is CVBS, component, VGA (analog RGB), HDMI, DVI video signals, etc., OLED Display requires an external video decoder, such as ADV7180, AD9985, ADV7611 and so on.

3.1.1 Input Video Standard

Table 3-1 Input Signal Standard & Pin Used

Video Standard	Color Space	PIN		
		R[7:0]	G[7:0]	B[7:0]
8-bit, 4:2:2	YCbCr	-	YCbCr[7:0]	-
8-bit, Mono	Y	-	Y[7:0]	-
16-bit, 4:2:2	YCbCr	-	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]

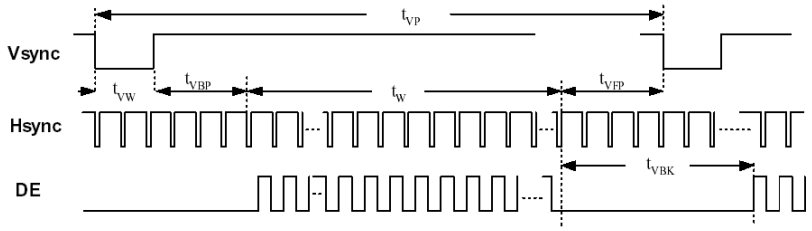


Figure 3-2 Input Sync Signals Timing (For All Formats)

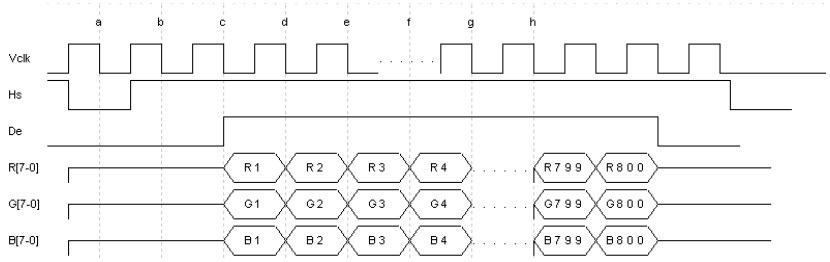


Figure 3-3 24-bit, 4:4:4 RGB Input VideoTiming

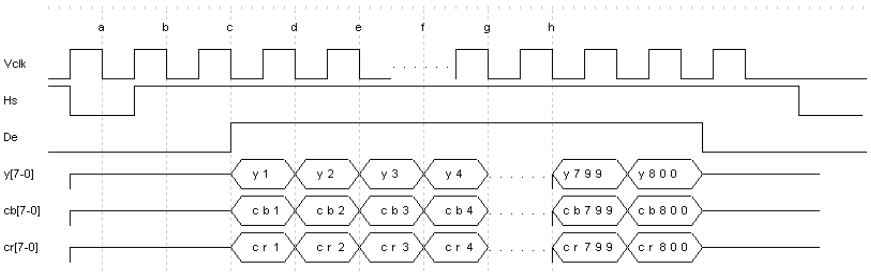


Figure 3-4 24-bit, 4:4:4 YCbCr Input Video Timing

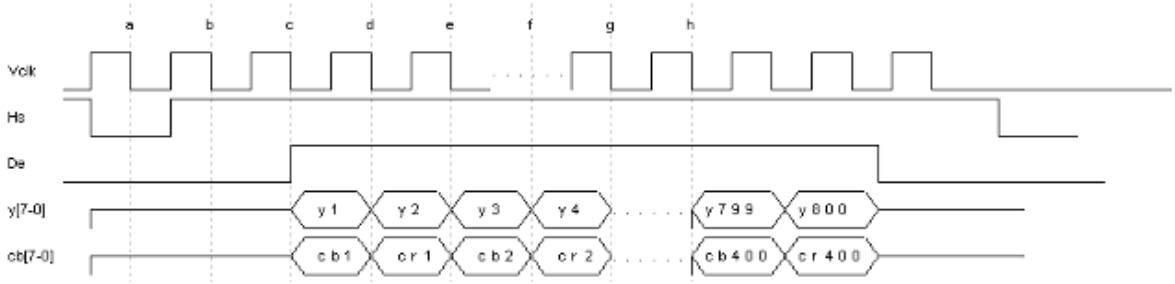


Figure 3-5 16-bit, 4:2:2 YCbCr Input Video Timing

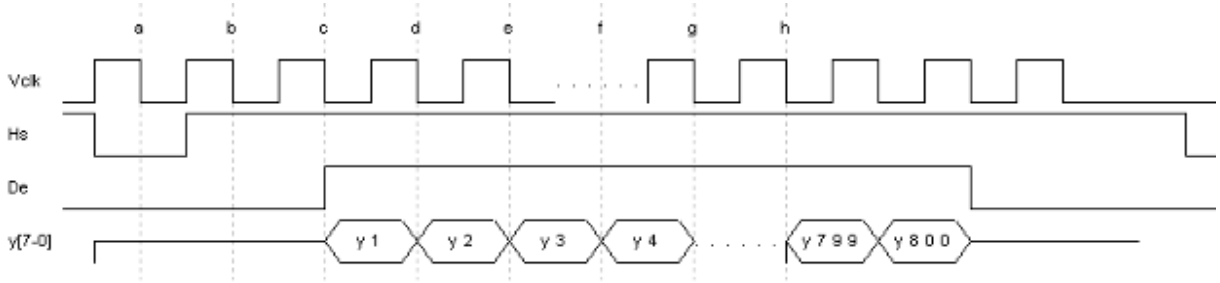


Figure 3-6 8-bit, Mono Input Video Timing

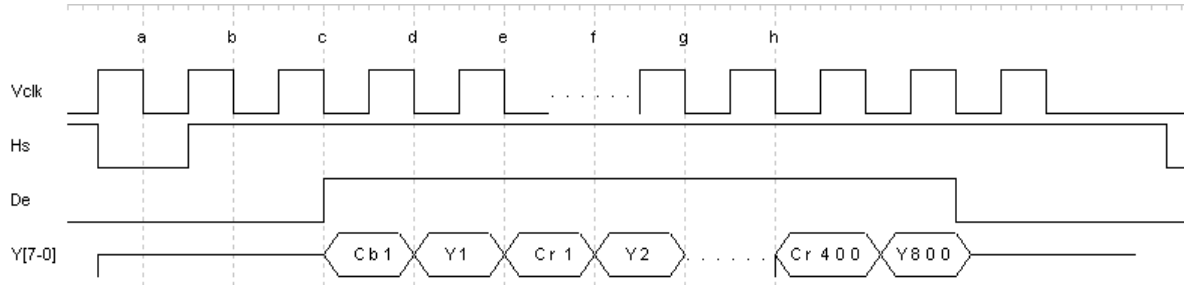


Figure 3-7 8-bit, 4:2:2 YCbCr input Video timing

Table 3-2 VESA Progressive Video Modes

Mode		Frequency	Total	Active	Front Porch + Border	Sync Pulse	Back Porch + Border
WVGA 800X480 85Hz non-interlaced	H	29.82 KHz	992 pixels	800 pixels	16 pixels	80 pixels	96 pixels
	V	60.000 Hz	497 lines	480 lines	1 line	3 lines	13 lines
	P	33.000 MHz					
VGA 640X480 85Hz non-interlaced	H	43.269 KHz	832 pixels	640 pixels	56 pixels	56 pixels	80 pixels
	V	85.008 Hz	509 lines	480 lines	1 line	3 lines	25 lines
	P	36.000 MHz					
VGA 640X480 75Hz non-interlaced	H	37.500 KHz	840 pixels	640 pixels	16 pixels	64 pixels	120 pixels
	V	75.000 Hz	500 lines	480 lines	1 line	3 lines	16 lines
	P	31.500 MHz					
VGA 640X480 60Hz non-interlaced	H	31.469 KHz	800 pixels	640 pixels	16 pixels	96 pixels	48 pixels
	V	59.940 Hz	525 lines	480 lines	10 line	2 lines	33 lines
	P	25.175 MHz					

Table 3-3 VESA Interlaced Video Modes

Mode		Frequency	Total	Active
SMPTE-170M-1 640X480 Mono 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.27 MHz		
NTSC 720X480 Color 30Hz interlaced	H	15.734 KHz	858 pixels	720 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	13.5 MHz		
NTSC (Square) 640X480 Color 30Hz interlaced	H	15.734 KHz	780 pixels	640 pixels
	V	60 Hz Field	262.5 lines	240 lines
	P	12.2727 MHz		

Table 3-4 VGA and WVGA Video Timing

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	f_{CLK}		33		MHz	WVGA 60Hz
HSYNC Period	t_{HP}	670			t_{CLK}	
HSYNC Pulse Width	t_{HW}	10			t_{CLK}	
HSYNC Back Porch	t_{HBP}	10			t_{CLK}	
Horizontal Valid data width	t_{HV}	640		800	t_{CLK}	
HSYNC Front Porch	t_{HFP}	10			t_{CLK}	
Horizontal Blank	t_{HBK}	30			t_{CLK}	
VSYNC Period	t_{VP}	243			t_{HP}	
VSYNC Pulse Width	t_{VW}	1			t_{HP}	
VSYNC Back Porch	t_{VBP}	1			t_{HP}	
Vertical valid data width	t_{W}	240		480	t_{HP}	
Vertical Front Porch	t_{VFP}	1			t_{HP}	
Vertical Blank	t_{VBK}	3			t_{HP}	

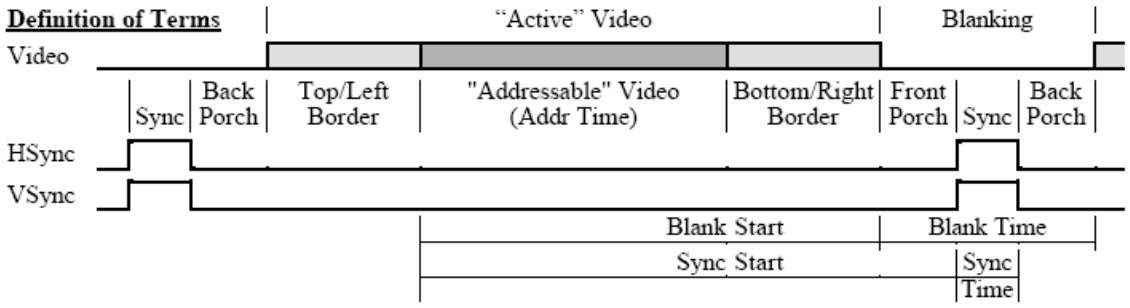


Figure 3-8 VESA Definition of Terms

3.1.2 Color Space

If the input data format is YCbCr, the device will change it to RGB format. Color space conversion block converts color space from YCbCr to RGB and uses the following equations. Output signal is 24-bit RGB format, 8-bit in each path.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$

$$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$

$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$

3.1.3 Digital Video Signal Enhancement

Digital video signal enhancement can be achieved by adjusting the brightness and the contrast ratio, as is shown in Figure 3-9.

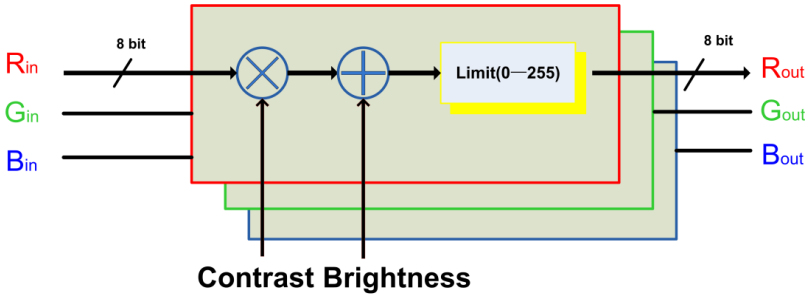


Figure 3-9 Digital Video Signal Enhancement Diagram

Brightness adjustment using addition and subtraction to achieve, the output value is equal to the input value plus the value of register 0EH, and then minus 128. When the value of register 0EH is greater than 80H, it means increase the brightness, whereas decrease. Brightness adjustment range is ±128.

$$V_{out} = V_{in} + Reg(0EH) - 128$$

Contrast adjustment using multiplication and division to achieve, the output value is equal to the input value multiplied by the value of register 0FH and then divided by 128. When the value of register 0FH is greater than 80H, it means increase the contrast, whereas decrease. The gain of contrast adjustment range is 0 to 2.

$$V_{out} = V_{in} \cdot \frac{Reg(0FH)}{128}$$

Note: The algorithms keep only 8bit data, if overflow, automatically discarded high bit.

3.1.4 Video Pattern Generation

Built-in test pattern generator can generate color bars, gray scale, tiles, horizontal stripes, vertical stripes, as well as monochrome red, *green*, blue, white, black and adjustable any R/G/B gray test pattern. Register 06H is pattern mode selection, default value is 0, indicates the test pattern generator is turned off; when select adjustable R/G/B gray pattern mode, registers 07H, 08H and 09H are used to set the 8-bit gray level of R/G/B channels respectively. Details of setting refer to Table 3-5 and Figure 3-10

Table 3-5 Summary of Test Pattern Setting

Register / Pattern	Mode (06H)	R (07H)	G (08H)	B (09H)
Color Bar	01H	—	—	—
Gray Scale	02H	—	—	—
Checker Board (40×40)	03H	—	—	—
Alternating every 2 rows	04H	—	—	—
Alternating every 2 columns	05H	—	—	—
All black	06H	—	—	—
All white	07H	—	—	—
All Red	08H	—	—	—
All Green	09H	—	—	—
All Blue	0AH	—	—	—
Adjustable RGB Gray①	0BH	0~255	0~255	0~255

Note① ： At adjustable RGB gray mode, the gray level range both are 0~255 (8-bit) of RGB channels. An 8-bit register is used to storing the 8-bit data.

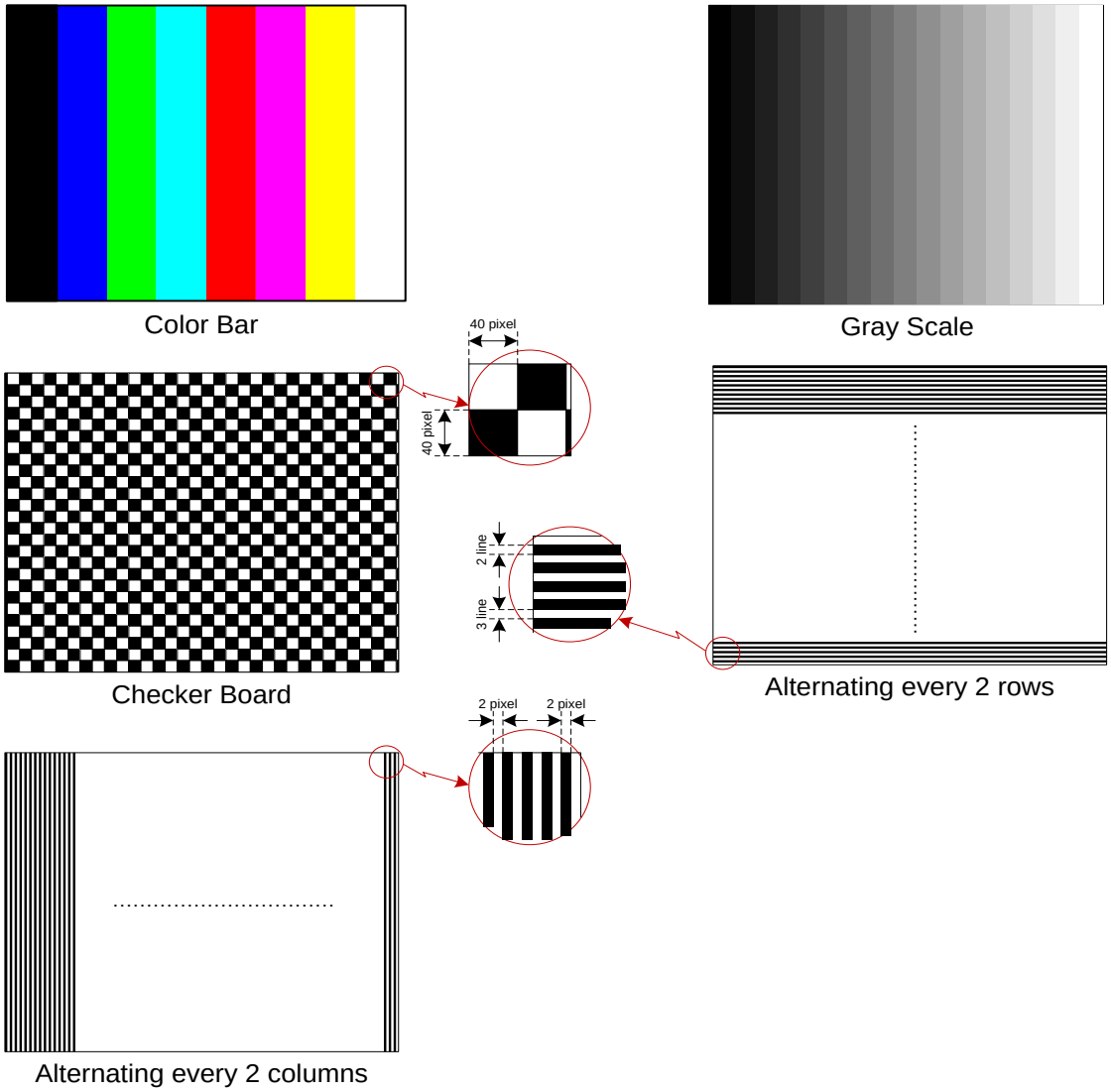


Figure 3-10 Test Video Patterns

3.1.5 Gamma Correction

WVGA series products integrate 3-channel RGB separate lookup table (LUT) to achieve high-precision gamma correction. Each LUT has 256-point, 8-bit input to 10-bit output resolution. Besides, WVGA also has a 14-point built-in Linear arithmetic.

At power-on default state, gamma correction is disabled, the LUTs were filled with random values. 8-bit input video data is directly sent to the MSB of 10-bit output bus, and the low 2-bit is set to 0. User needs to initializes the LUTs before enabled the gamma correction, otherwise there might be display irregularly.

The LUT's working is depended on the external input clock signal (VCLK), when the Reset pin is release (set to 1), wait at least 480 VCLK cycles before to operating the LUTs. If no VCLK, the LUT's operating does not have any error response, but the actual operating will not been performed, even to enabled the gamma correction.

The LUT's operating using a register groups and special timing, details refer to section 3.7.3.

3.2 3D Video Display

Register 20H.bit1 used to enable the 3D function and 20H.bit0 used to set the polarity of 3D input signal, cooperated with 3D pin's input (Pin9), the 3D video display can be achieved. If 3D pin's input level is same as the setting of 20H.bit0, the video input is valid, and the frame/field video will be updated, otherwise, video input is invalid and the display will keep the current frame/field. 3D pin's signal is latched at VS falling edge. 3D video display timing is shown in Figure 3-11.

In progressive mode, 3D video signal using frame timing mode, such as the odd frame is updated left display, and the even frame is updated right display.

In interlaced mode, 3D video signal using field timing mode, such as the odd field is updated left display, and the even field is updated right display. At this point, the vertical resolution of each field is lower compare with the source, the bit5 and bit4 of register(02H) should be set to "11", display will repeat to display each line in next line automatically, to ensure that the image aspect ratio and display.

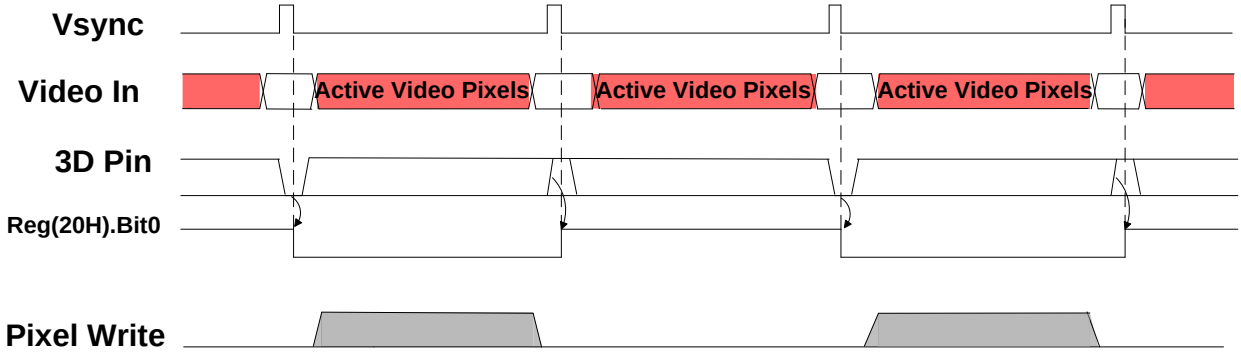


Figure 3-11 3D Video Display Timing

3.3 Power Supply & Reset

WVGA041S need 5V&1.8V power supply. The 1.8V is used for digital core. 5V is used for OLED pixels driver, D/A converter and DC-DC module. To ensure the display image quality, please note that ripple and noise rejection of 5V power supply.

3.3.1 Power UP/Down Sequence

The system power-up mechanism relies on the clock signal (VCLK), so the power supply and VCLK input sequence is very important. WVGA041S requires first provide VCLK, followed is 1.8v, and last is 5V. The working principle is shown by following figures and section 3.3.2.

If the power-up sequence cannot meet requirements, WVGA041S's working state may abnormal. In that case, after the reset and initialization operations, user can set the PDOWN (Register 50H.Bit7) to 1 first, and wait 20ms, then set PDOWN to 0.

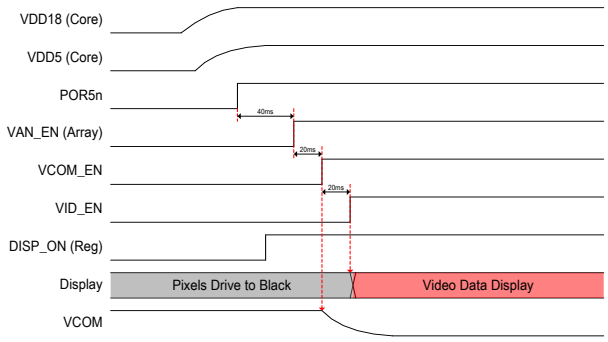


Figure 3-12 Power-up Sequence ($V_{th_1.8}$=1.2V)

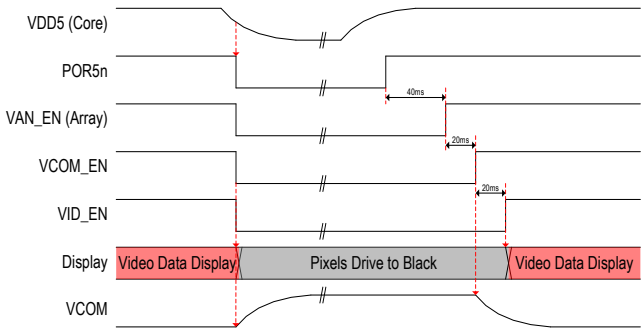


Figure 3-13 V5.0 Power Down & Up (Vth=4V)

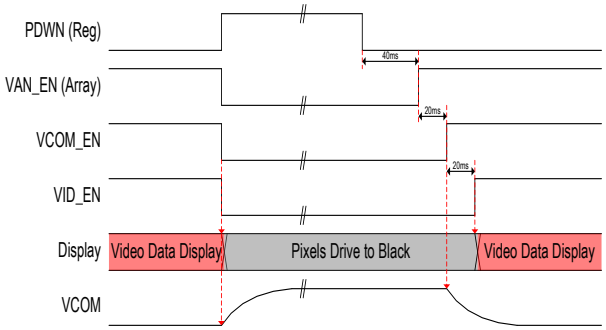


Figure 3-14 Register Control Power Down & Up

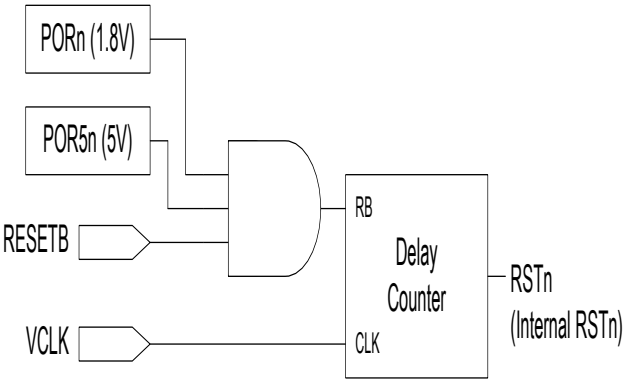


Figure 3-15 Reset Block Diagram

3.3.2 Reset Sequence

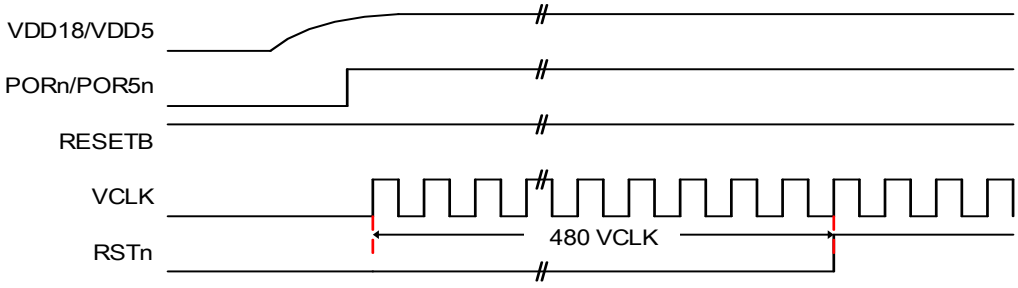


Figure 3-16 Reset Timing Case 1 – No external reset pin used (RESETB=1)

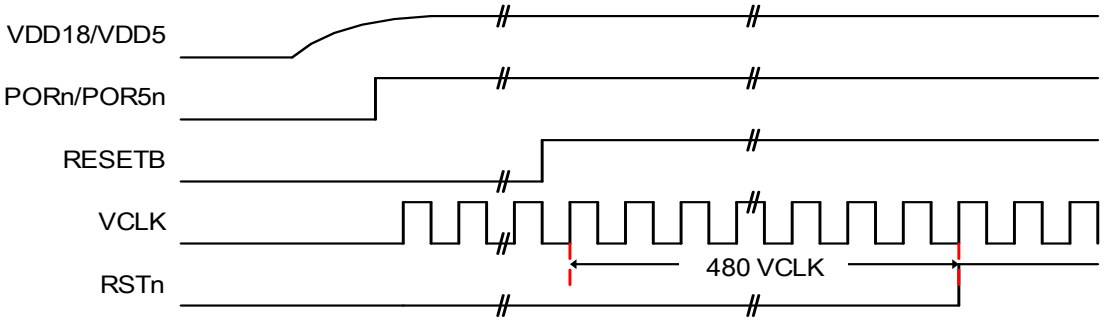


Figure 3-17 Reset Timing Case 2 – External reset pin depend on VCLK

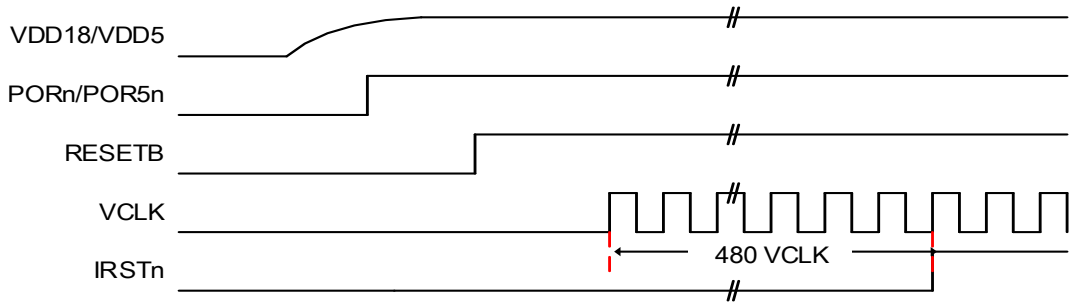


Figure 3-18 Reset Timing Case 3 – External reset pin applied

3.4 Unit Drive Circuit

WVGA041S series AMOLED pixel drive circuit is shown in Figure 3-19. Each OLED light-emitting diodes use voltage-driven approach, the typical photo electric properties is shown in Figure 3-20.

When scanning signals ROWSEL and ROWSWL_B are valid at the same time, signal Video_In charges the capacitance C through MOS transistors P1&N1, and controls the output of N2. The capacitance C can be guaranteed to maintain the output of N2 in a frame/field cycle.

N2 is used in Source-Follower structure to control 5V (Van) power supply, the current flowed through the protection resistor R is applied to the OLED anode.

All pixels cathode of OLED is connected to negative voltage Vcom (common cathode structure), Vcom can be adjusted by set 9-bit registers 44:45H in order to achieve the display brightness adjustment.

N3 is used for discharge of parasitic capacitance of the OLED rapidly, thereby improving dynamic contrast of the display. The discharge enabled by register 42H.bit1.

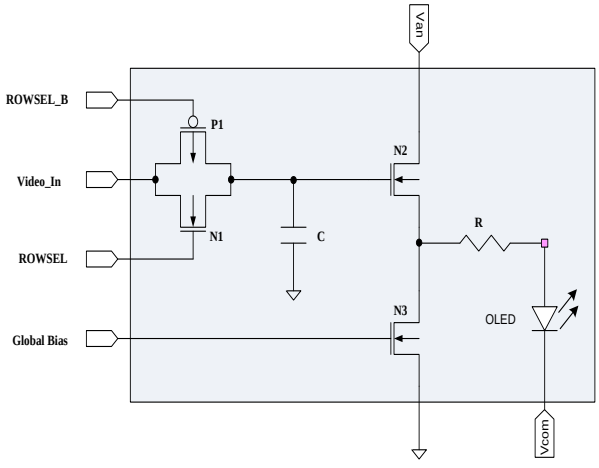


Figure 3-19 Unit Drive Circuit

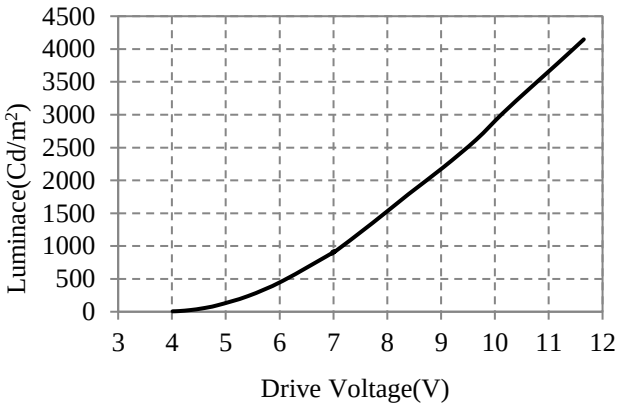


Figure 3-20 OLED photo electricity properties

3.5 DC/DC Converter

OLED emitting light needs to be applied positive bias voltage between the anode and cathode, the anode voltage

from 5V power supply is controlled by drive transistor, all pixel's common cathode voltage Vcom supplied by DC/DC converter on the PCB backplane. The driving pulse of DC/DC converter is generated by the internal programmable pulse generator, the circuit shown in Figure 3-21. Vcom adjustment range is 0 ~-3V, corresponding to 9-bit registers 44:45H, the typical working curve is shown in Figure 3-22.

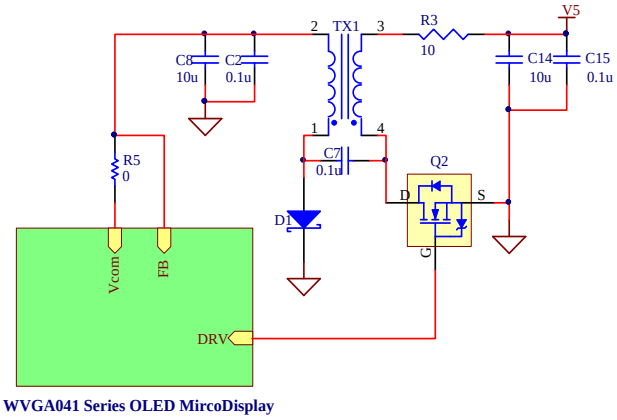


Figure 3-21 DC/DC Principal Diagram

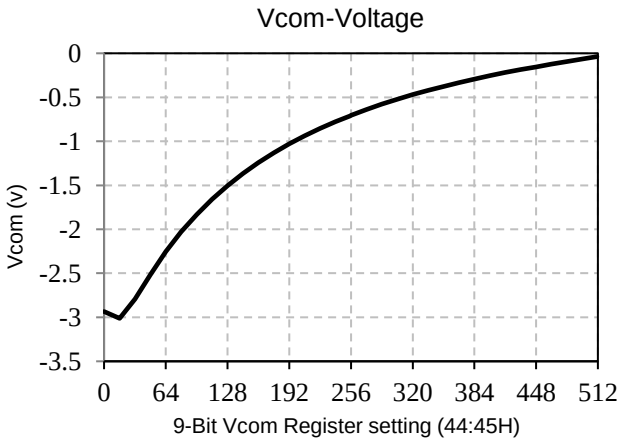


Figure 3-22 Vcom Programmable Working Curve

3.6 Temperature Sensor

The working of WVGA041S's temperature sensor depend on external VS signal, and the measured value update period is 256 cycles of VS signal (if VS=60Hz, it's about 4.3s).

The value of register 4AH is the measured value of internal temperature sensor. So the real-time internal working temperature can be read out through the two-wire serial interface. The temperature value and the readout conversion relation is: $T = 0.47 \times \mathrm{Reg}\,(4AH) - 40$

The temperature sensor response curve and the calibration curve are shown as Figure 3-23 and Figure 3-24.

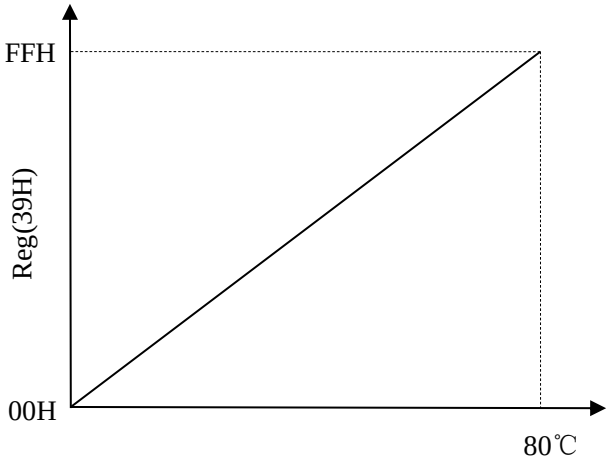


Figure 3-23 Temp. Sensor Readout

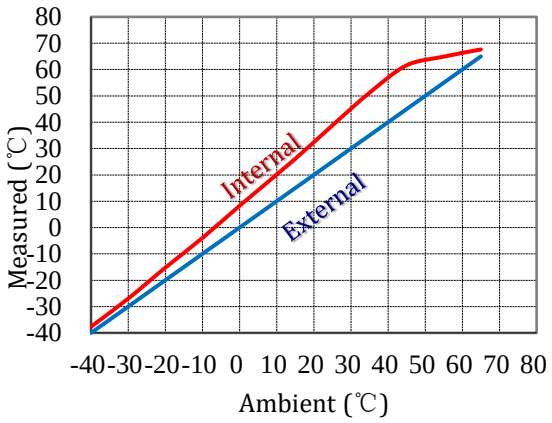


Figure 3-24 Temp. Sensor calibration curve

3.7 IIC Interface

WVGA041S's IIC interface compatible only with the random address read/write operations of IIC communication standard. WVGA041S series microdisplay acts as a slave for receiving and transmitting data, all read/write operations must be launched by the master. The SDA and SCL line has been pulled up to internal 1.8v via 10k resistor.User can realize the display programmable control by use IIC interface, such as digital video signal decoding and processing, gamma correction, Vcom adjustment and so on.

Key Features and tags of the two-wire serial communication:

1) Communication speed (SCL) support from 100K to 1MHz;
2) 8-bits Slave Address consists of 7-bits device address and 1-bit read/write flag;
3) Start/Re-Start: SDA change from HIGH to LOW while SCL is HIGH, See Figure 3-25;
4) Stop: SDA change from LOW to HIGH while SCL is HIGH, see Figure 3-25;
5) ACK: SDA is LOW during the acknowledge clock pulse;
6) NAK: SDA is HIGH during the acknowledge clock pulse;
7) One transmission includes 8bit data and an acknowledge bit, total nine clock of SCL;
8) Except Start and Stop condition:
   - HIGH or LOW state of SDA can only being changed while SCL is LOW
   - Data on the SDA line must be stable during the HIGH period of the SCL

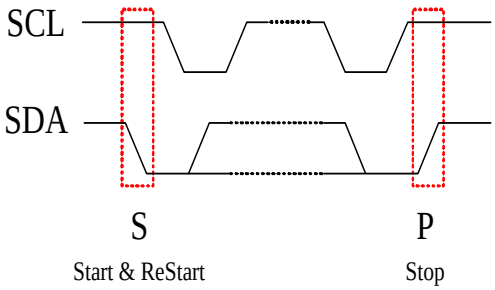


Figure 3-25 Start & Stop Timing

3.7.1 Communication Operating

- Write data (Figure 3-26) :
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents as low
  3) Slave sends 1bit ACK (A) response
  4) Master sends 8bit register address (Register)
  5) Slave sends 1bit ACK (A) response
  6) Master sends 8bit data (Data)
  7) Slave sends 1bit ACK (A) response
  8) Master sends stop condition(P)

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 3-26 Write Data format

- Read Data (Figure 3-27)
  1) Master sends Start condition (S)
  2) Master sends 7bit Slave Address and 1bit Write flag ($\overline{W}$) represents as low
  3) Slave sends ACK (A) response

4) Master sends 8bit Register Address (Register)
5) Slave sends 1bit ACK (A) response
6) Master sends 1bit Re-Start condition (Sr)
7) Master sends 7bit Slave Address and 1bit Read flag (R) represents as high
8) Slave sends 1bit ACK (A) response
9) Slave sends 8bit Data (Data)
10) Master sends 1bit NAK ($\overline{A}$) response
11) Master sends Stop condition (P)

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P

Figure 3-27 Data format (Master reads from Slave)

3.7.2 IIC Address Selection

Two salve address of WVGA041S series microdisplay can be selected by SelAdr0 pin. The SelAdr0 pin has an internal resistor (10K) to pull up to 1.8V power. One of microdisplay's SelAdr0 pin must be connected to GND when used in binocular stereovision application. Microdisplay's corresponding read/write address is shown as Table 3-6.

Table 3-6 Slave Address list

A7 (MSB)	A6	A5	A4	A3	A2	A1 (SelAdr0)	A0 (R/$\overline{W}$)	Slave Address (R/$\overline{W}$)
0	0	0	1	1	1	1(Default)	1/0	1FH/1EH
0	0	0	1	1	1	0	1/0	1DH/1CH

3.7.3 Gamma LUT operation

WVGA041S integrate 3-channel RGB separate lookup table (LUT), and each LUT has 256-point, 10-bit resolutions, so the LUTs addressing rang beyond 8-bit. WVGA041S was using a register groups and special timing to achieve the LUTs operation by indirect addressing mode. The register group definition refers to Table 3-7

Table 3-7 The register group of Gamma function

Channel	LUT Addressing Register	LUT Data Register		Control Register(20H)		
		MSB_Data[9:8]	LSB_Data[7:0]	En	Read	Update
Red	21H	22H	23H	Bit7	Bit6	Bit2
Green	24H	25H	26H		Bit5	Bit1
Blue	27H	28H	29H		Bit4	Bit0

- Write LUT (Example as R channel)
  1) Check 20H.Bit2 = 0;
  2) Initialiation the gamma correction RedData(0~255), Addr=0;
  3) Write the Addr to 21H;
  4) Write RedData(Addr)_[9:8] to 22H & Write RedData(Addr)_[7:0] to 23H;
  5) LUT_Red[Addr] = RedData(Addr)
  6) Addr=Addr+1;
  7) repeat 3~6, until Addr=255;
  8) Set 20H.Bit2=1; //Updating the LUT_Red

** After 3-channel (RGB) has been updating, set 20H.Bit2 to enable the gamma correction.*

- Read LUT (Example as R channel)
  1) Check 20H.Bit6 = 0;
  2) Define arrays ready to receive data; //RData(256)
  3) Addr=0;
  4) Write Addr to 11H
  5) Set 20H.Bit6=1; //Start Reading
  6) wait 20H.Bit6=0; //Data Ready
  7) Read 22H to RData(Addr)_[9:8] & Read 23H to RData(Addr)_[7:0]; // Get RData(Addr)
  8) Addr=Addr+1;
  9) Repeat 4~9, until Addr=255;

3.8 Three-wire SPI Interface

WVGA041S's Three-wire SPI Interface use the same data & clock line as its IIC interface. When SPICS pin is pulled-down, SPI mode is enabled, otherwise the IIC mode is enabled. Please refer to the Timing (Figure 3-28).

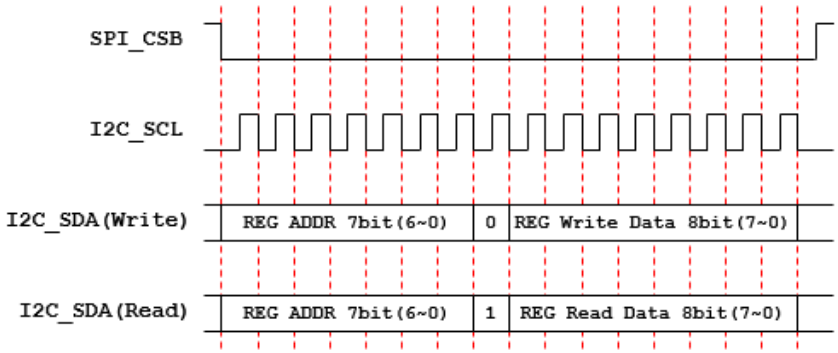


Figure 3-28 Three-wire SPI Timing

- Write Data (Figure 3-29)
  - Master pull down the SPI_CSB;
  - Master send the target register address: (Reg(Addr) < 1) & 0xFE;
  - Master send the data.

$\overline{\text{SPI_CSB}}$		Reg Addr(7 bit)	0		Data(8 bit)

Figure 3-29 3-Wire SPI write data

- Read Data (Figure 3-30)
  1) Master pull down the SPI_CSB;
  2) Master send the target register address: (Reg(Addr) < 1) | 0x01;
  3) Master read the data.

$\overline{\text{SPI_CSB}}$		Reg Addr(7 bit)	1		Data(8 bit)

Figure 3-30 3-Wire SPI read data

4 REGISTER DESCRIPTION

4.1 Summary of Registers

Table 4-1 Summary of Registers

Register	Bytes	Description	Default Value
00H	1	Chip's Revision	30H
01H	1	Video Signal Setting	03H
02H	1	Video Mode Setting	43H
03H	1	Vertical Blank Lines Setting	00H
04H	1	Horizontal Blank Pixels Setting	00H
06H	1	Test Pattern Enable and Mode Setting	00H
07H	1	R Channel 8-bit Gray Setting for Pattern Mode(0BH)	00H
08H	1	G Channel 8-bit Gray Setting for Pattern Mode(0BH)	00H
09H	1	B Channel 8-bit Gray Setting for Pattern Mode(0BH)	00H
0EH	1	Video Signal Brightness Control	80H
0FH	1	Video Signal Contrast Control	80H
10H	1	Linear Gamma Function Control	80H
11H	1	R Channel offset value	60H
12H	1	G Channel offset value	60H
13H	1	B Channel offset value	60H
14H	1	Point 0 value of Linear Gamma	05H
15H	1	Point 1 value of Linear Gamma	09H
16H	1	Point 2 value of Linear Gamma	10H
17H	1	Point 3 value of Linear Gamma	1BH
18H	1	Point 4 value of Linear Gamma	30H
19H	1	Point 5 value of Linear Gamma	43H
1AH	1	Point 6 value of Linear Gamma	54H
1BH	1	Point 7 value of Linear Gamma	74H
1CH	1	Point 8 value of Linear Gamma	93H
1DH	1	Point 9 value of Linear Gamma	AFH

Register	Bytes	Description	Default Value
1EH	1	Point 10 value of Linear Gamma	CBH
1FH	1	Point 11 value of Linear Gamma	E6H
20H	1	Gamma LUTs Function Control	00H
21H	1	R Channel LUTs Address	00H
22:23H	2	R Channel LUTs Data[9:0]	000H
24H	1	G Channel LUTs Address	00H
25:26H	2	G Channel LUTs Data[9:0]	000H
27H	1	B Channel LUTs Address	00H
28:29H	2	B Channel LUTs Data[9:0]	000H
30H	1	3D Mode Control	00H
31H	1	Display Mode Control	00H
33H	1	Left Margin Control	02H
35H	1	Right Margin Control	02H
37H	1	Top Margin Control	02H
39H	1	Bottom Margin Control	02H
40H	1	DAC Output Slope Control	D8H
41H	1	DAC Current Control	04H
42H	1	DAC Output Control	00H
43H	1	DC-DC Output Control	42H
44:45H	2	Vcom Output Control	1FFH
4AH	1	Temperature Value	-
50H	1	Power Down Control	08H

4.2 Detailed Information of Registers

Table 4-2 Detailed information of registers

Category	Register	R/W	Bit	Function	Default	Description
Revision	00H	R	7:4	Product	0011b	0001b : SXGA 0010b : WUXGA 0011b : WVGA
			3:0	Revision	0000b	0000b : Revision Number

Category	Register	R/W	Bit	Function	Default	Description
Input Video Control	01H	R/W	7	Data Mode	0b	0b : 24/16/8-bit SDR mode 1b : Reserved (Must be set to 0)
			3	Vsync Polarity	0b	0b : Active High 1b : Active Low
			2	Hsync Polarity	0b	
			1:0	Sync Mode	11b	00b : Embedded Sync 10b : External Sync without DE 11b : External Sync wity DE
Input Video Control	02H	R/W	7:6	SAV Offset	01b	00b : 1 Pixel before Input SAV 01b : Same as Input SAV 10b : 1 Pixel after Input SAV 11b : 2 Pixel after Input SAV
			5:4	Interlace Mode	00b	00b : Progressive 10b : Interlaced1 11b : Interlaced2 (for Field 3D)
			2:0	Data Format	011b	000b : 16-bit 422 YCbCr 001b : 24-bit 444 YCbCr 010b : 8-bit Mono 011b : 24-bit 444 RGB 100b : 8-bit 422 YCbCr
	03H	R/W	7:0	V Blank	00H	Vertical Blank Lines
	04H		7:0	H Blank	00H	Horizontal Blank Pixels
Test Pattern Control	06H	R/W	3:0	Test Pattern Mode	00H	0H : Normal (Test Pattern Closed) 1H : Color Bar 2H : Gray Scale 3H : Checker Board (40×40) 4H : Alternating every 2 Rows 5H : Alternating every 2 Columns 6H : All Black 7H : All White 8H : All Red 9H : All Green AH : All Blue BH : Adjusted R/G/B (Any Gray Level)
	07H	R/W	7:0	TP Red [7:0]	00b	R Channel 8-bit Gray Value
	08H		7:0	TP Green [7:0]	00b	G Channel 8-bit Gray Value
	09H		7:0	TP Red [7:0]	00b	B Channel 8-bit Gray Value
Video Enhancement	0EH	R/W	7:0	Brightness	80H	00H : Darkest 80H : No Change FFH : Brightest
	0FH	R/W	7:0	Contrast	80H	00H : Black Screen 80H : No Change FFH : Double Contrast
Linear Gamma Control	10H	R/W	7:0	Linear Gamma Bypass	1b	0 : Linear Gamma Enable 1 : Liner Gamma Disable
				Update	0b	Update Enable & Status 0 : Update Done 1 : Update Start (Automatic clear)
	11H	R/W	7:0	R Offset	60H	Red Offset Value for Linear Gamma
	12H	R/W	7:0	G Offset	60H	Green Offset Value for Linear Gamma
	13H	R/W	7:0	B Offset	60H	Blue Offset Value for Linear Gamma

Category	Register	R/W	Bit	Function	Default	Description
Linear Gamma Control	14H	R/W	7:0	Point 0	05H	Point 0 Value for Linear Gamma
	15H	R/W	7:0	Point 1	09H	Point 1 Value for Linear Gamma
	16H	R/W	7:0	Point 2	10H	Point 2 Value for Linear Gamma
	17H	R/W	7:0	Point 3	1BH	Point 3 Value for Linear Gamma
	18H	R/W	7:0	Point 4	30H	Point 4 Value for Linear Gamma
	19H	R/W	7:0	Point 5	43H	Point 5 Value for Linear Gamma
	1AH	R/W	7:0	Point 6	54H	Point 0 Value for Linear Gamma
	1BH	R/W	7:0	Point 7	74H	Point 0 Value for Linear Gamma
	1CH	R/W	7:0	Point 8	93H	Point 0 Value for Linear Gamma
	1DH	R/W	7:0	Point 9	AFH	Point 0 Value for Linear Gamma
	1EH	R/W	7:0	Point 10	CBH	Point 0 Value for Linear Gamma
	1FH	R/W	7:0	Point 11	E6H	Point 0 Value for Linear Gamma
Gamma LUTs Control	20H	R/W	7	LUTs Bypass	1b	0b : LUTs Enable 1b : LUTs Disable
			6	R LUTs Read	0b	0b : Read Done 1b : Read Start (Automatic Clear after Read)
			5	G LUTs Read	0b	
			4	B LUTs Read	0b	
			2	R LUTs Update	0b	0b : Update Done 1b : Update Start (Automatic Clear after Update)
			1	G LUTs Update	0b	
			0	B LUTs Update	0b	
	21H	R/W	7:0	R _LUTs_ Address	00H	Read/Write Address for Red Gamma LUTs
	22H		1:0	R_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Red Gamma LUTs
	23H		7:0	R_LUTs_Data[7:0]	00H	
	24H		7:0	G _LUTs_ Address	00H	Read/Write Address for Green Gamma LUTs
	25H		1:0	G_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Green Gamma LUTs
	26H		7:0	G_LUTs_Data[7:0]	00H	
	27H		7:0	B _LUTs_ Address	00H	Read/Write Address for Blue Gamma LUTs
	28H		1:0	B_LUTs_Data[9:8]	00b	Read/Write Data[9:0] for Blue Gamma LUTs
	29H		7:0	B_LUTs_Data[7:0]	00H	
3D Function	30H	R/W	1	3D Mode	0b	0b : Disable 1b : Enable

Category	Register	R/W	Bit	Function	Default	Description
			0	3D Polarity	0b	0b : Active when 3D pin is Low 1b : Active when 3D pin is High
Display Control	31H	R/W	7	Display On	0b	0b : Display Off 1b : Display On
			4	Display Enable	1b	0b : Disable (Only IIC&SPI work) 1b : Enable(Must be set 1 after configuration)
			1	Horizontal Mirror	0b	0b : Disable (Left to Right, Top to Bottom)
			0	Vertical Mirror	0b	1b : Enable (Right to Left, Bottom to Top)
	33H	R/W	7:0	Left Margin [7:0]	0b	Display Left Margin [8:0]
	35H		7:0	Right Margin [7:0]	02H	
	37H		7:0	Top Margin [7:0]	0b	Display Right Margin [8:0]
	39H		7:0	Bottom Margin [7:0]	02H	
DAC Control	40H	R/W	7:0	DAC Slope	D8H	Adjust DAC Output Slope
	41H	R/W	2:0	DAC Current	100b	Adjust DAC Current
	42H	R/W	2	DAC MAX	0b	0b : VCLK 1b : Internsal OSC
			1	DAC Discharge	0b	0b : Slow 1b : Fast
			0	DAC Monitor	0b	0b : Disable 1b : Enable
Vcom Control	43H	R/W	7	DC-DC Select	0b	0b : VCLK 1b : Internal Ring OSC
			6:4	DC-DC Duty	100b	000 : 1:7 001 : 2:6 010 : 3:5 011 : 4:4 100 : 5:3 101 : 6:2 110 : 7:1
			2:0	DC-DC Divide	010b	000 : 8 001 : 16 010 : 32 011 : 64 100 : 128 101 : 256 110 : 512 111 : 1024
Vcom Level	44H	R/W	0	VcomLevel [8]	1b	Programble Vcom Level [8:0]
	45H		7:0	VcomLevel [7:0]	FFH	
Temperature	4AH	R	7:0	Temperature Value	0～FFH	Temperature Output Value
Power Down Mode	50H	R/W	7	PD All	0b	0b : Normal 1b : Power-Down
			2	PD DAC	0b	
			1	PD Vcom	0b	
			0	PD Temperature Sensor	0b	

4.3 Register Setting Examples

4.3.1 24 bit 444 RGB with DE Mode

Table 4-3 Display configuration example

Register	Setting	Description
01H	03H	SDR Mode, VSync&HSync active high, External Sync with DE
02H	43H	Same as SAV, Progressive, 24Bit 444 RGB
33H	02H	Left Margin = 2
35H	02H	Right Margin = 2
37H	02H	Top Margin = 2
39H	02H	Bottom Margin = 2
44:45H	0F0H	Vcom Setting
31H	80H	Enable Display
10H	00H	Enable Linear Gamma
31H	90H	Turn the Display

4.3.2 Display Position Setting

Left Margin = Right Margin = (804 – X_Resolution) / 2

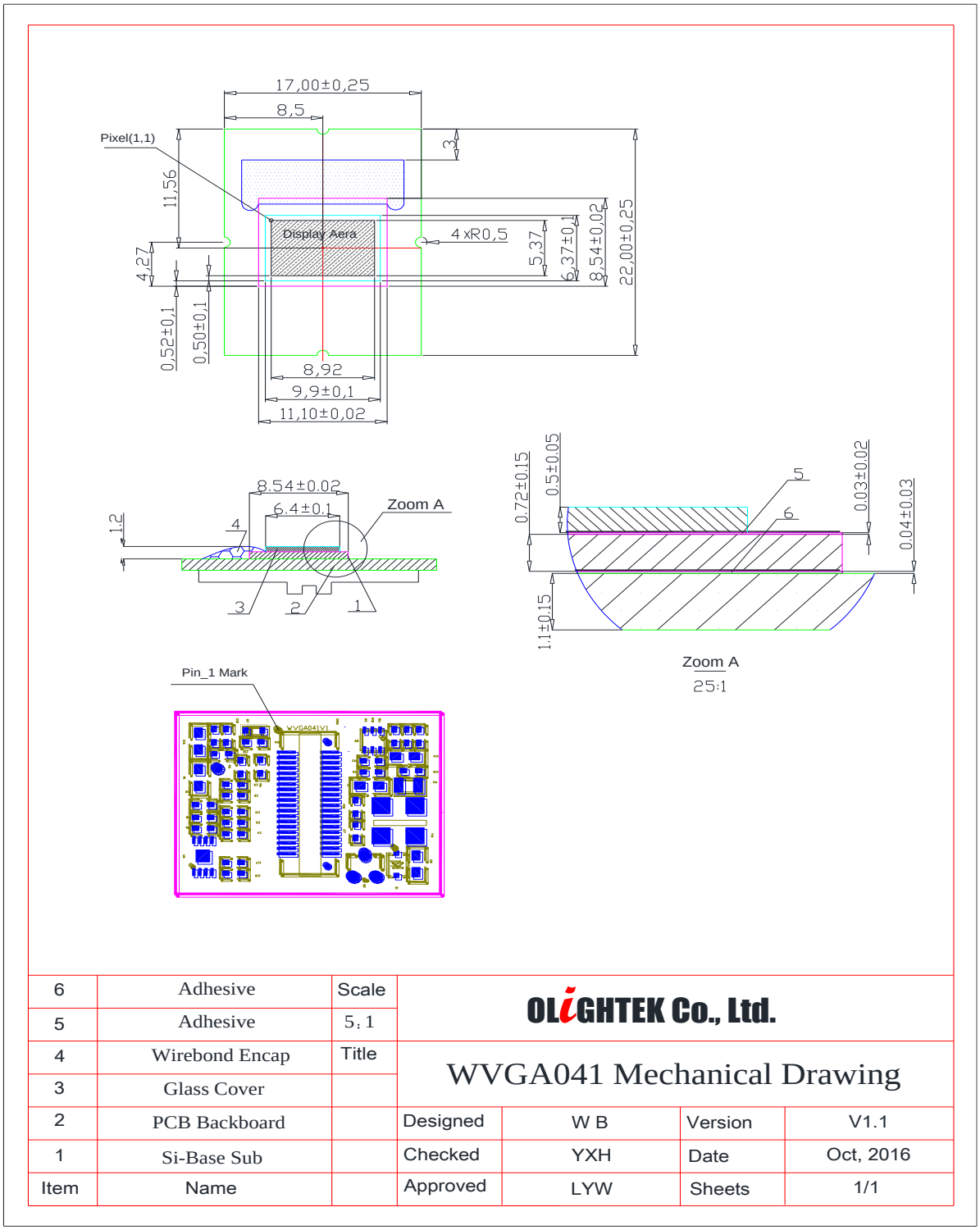
Top Margin = Bottom Margin = (484 – Y_Resolution) / 2

Table 4-4 Display Position Setting Example

Video Mode				Register Setting					
Mode	**Scan**	**Input**	**Display**	**Reg(01H)**	**Reg(07H)**	**Reg(11h)**	**Reg(12H)**	**Reg(13H)**	**Reg(14H)**
WVGA	Progressive	800×480	800×480	3CH	00H	02H	02H	02H	02H
VGA	Progressive	640×480	640×480	3CH	00H	52H	52H	02H	02H
SMPTE-170M-1	Interlaced	640×480	640×480	21H	00H	52H	52H	02H	02H
NTSC	Interlaced	720×480	640×480	41H	04H	2AH	2AH	02H	02H

5 MECHANICAL CHARACTERISTICS

5.1 Mechanical Drawing



6	Adhesive	Scale	OLIGHTEK Co., Ltd.			
5	Adhesive	5：1				
4	Wirebond Encap	Title	WVGA041 Mechanical Drawing			
3	Glass Cover					
2	PCB Backboard		Designed	W B	Version	V1.1
1	Si-Base Sub		Checked	YXH	Date	Oct, 2016
Item	Name		Approved	LYW	Sheets	1/1

Figure 5-1 Mechanical Drawing

5.2 PCB Backboard Schematic

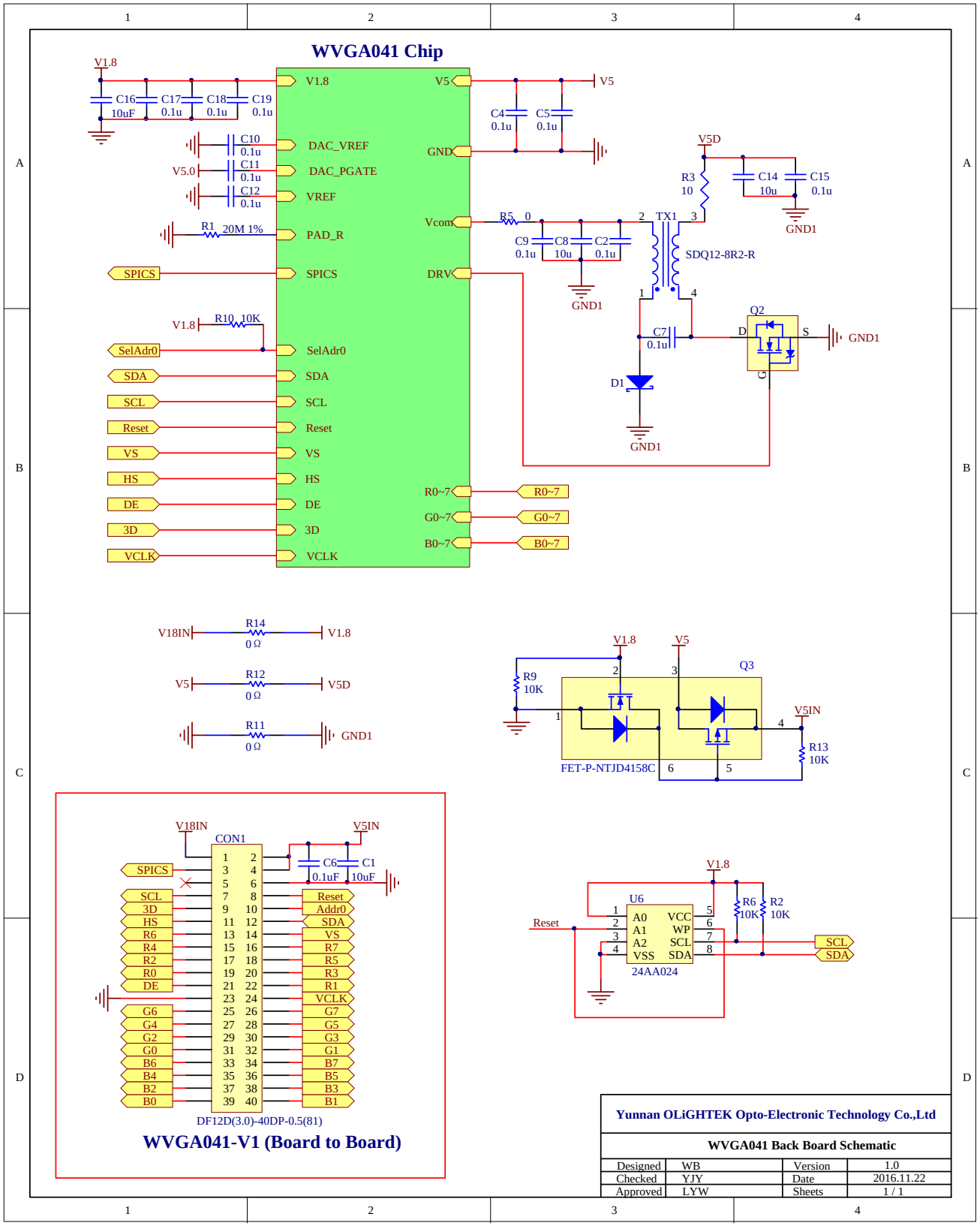


Figure 5-2 PCB Backboard Schematic

5.3 Assembly Bill of Materials

Table 5-1 Assembly Bill of Materials

No	Type	Reference	Qty	Description	Coding	Manufacturer
1	Cap	C2,C4,C5,C6,C7,C9,C10, C11,C12,C15,C17,C18,C19	13	Cap,0.1μF/25V,X5R,0402	TMK105BJ104KV-T	TAIYO YUDEN
		C1,C8,C14,C16	4	Cap,10μF/16V,X5R,0603	EMK212BJ106KG-T	TAIYO YUDEN
2	Diode	D1	1	Schottky Diode, 30V/1.5A,SOD323F	PMEG3015EJ	PHILIPS
3	Connector	CON1	1	Connector,40Pin,0.5mm,Header	DF12D(3.0)-40DP-0.5V	Hirose
4	N-FET	Q2	1	N-FET,20V/0.9A,SOT-23	FDV305N	Fairchild
5	FET	Q3	1	P-FET+N-FET 215+1000mohm,0.27W,SOT-363	NTJD4158C	ONSEMI
6	Resiter	R2,R6,R9,R10,R13	5	Resistor, 10K, 5% 1/16W,0402	RC0402JR-0710KL	YAGEO
		R3	1	Resistor, 10Ω, 5% 1/4W,0805	RC0805JR-0710RL	YAGEO
		R5,R11,R12,R14	4	Resistor, 0Ω, 5% ,0402	RC0402JR-070RL	YAGEO
		R1	1	Resistor, 20M, 1% ,0603	RS03M206FT	FengHua
7	Transformer	TX1	1	Transformer,6.8μH/0.6A, 1:1	LPD4012-682ML	Coilcraft
8	EEPROM	U6	1	2K, I2C Serial EEPROM, DFN-8	24AA024	Microchip

6 PRODUCTS CLEANING, HANDLING AND STORAGE

6.1 Cleaning

- Avoid using any acid, alkali and organic solvent to clean or contact to the display
- Using the lens paper or clean cloth to clean the surface is recommend

6.2 General Handling Considerations

- Do not expose the display to strong acids, alkalis, or solvents.
- Do not expose the display surface to UV or other strong ionizing radiation.
- Do not using sharp objects to contact the glass and silicon regions of display.
- Avoid applying force to the any region except the PCB backplane, especially apply the force to the region of sealing, silicon edge and cover glass is not allowed.
- Avoid immersion of the display in any liquid.
- Handing with PVC clean gloves is recommended.

6.3 Static Charge Prevention

The microdisplay is sensitive to electro-static discharge due to integrated CMOS circuit in the display. The following measures are recommended to minimize ESD occurrences:

- Operate on a region which is equipped with electro-static eliminator, such as ionizing air blowers.
- Wear the anti-static wrist strap
- wear the non-chargeable clothes
- Keep away from charged region.

Figure 6-1 Display Handling

6.4 Storage

6.4.1 Short Term Storage

The display should be stored in a dry environment with temperature range from -50℃ to 90℃ for a short period(≤100hrs).

6.4.2 Long Term Storage

If the display is stored in such an environment with excessive heat or cold or moisture, the lifetime of display will be shorten, even the environment can cause permanent damage to the display. Recommended long-term storage condition as follows:

- Room temperature: 25℃±5℃
- Dry environment: dry nitrogen or vacuum sealing cabinet
- Static placing: avoid violent vibration

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