

General Description

FSMOS® MOSFET is based on Oriental Semiconductor's unique device design to achieve low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. The high V_{th} series is specially designed to use in motor control systems with driving voltage of more than 10V.

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

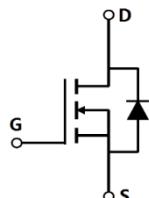
Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
I_D , pulse	800	A
$R_{DS(ON)}$, max @ $V_{GS}=10V$	1.9	mΩ
Q_g	144	nC

Marking Information

Product Name	Package	Marking
SFS08R019HNF	TO247	SFS08R019HN

Package & Pin information



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	350	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D,\text{pulse}}$	800	A
Continuous diode forward current ¹⁾ , $T_C=25^\circ\text{C}$	I_S	350	A
Diode pulsed current ²⁾ , $T_C=25^\circ\text{C}$	$I_{S,\text{pulse}}$	800	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	450	W
Single pulsed avalanche energy ⁴⁾	E_{AS}	735	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.33	$^\circ\text{C}/\text{W}$
Thermal resistance, junction-ambient	$R_{\theta JA}$	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	80			V	$V_{GS}=0 \text{ V}, I_D=250 \mu\text{A}$
Gate threshold voltage	$V_{GS(\text{th})}$	2		4	V	$V_{DS}=V_{GS}, I_D=250 \mu\text{A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		1.5	1.9	$\text{m}\Omega$	$V_{GS}=10 \text{ V}, I_D=30 \text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20 \text{ V}$
				-100		$V_{GS}=-20 \text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=80 \text{ V}, V_{GS}=0 \text{ V}$
Gate resistance	R_G		1.2		Ω	$f=1 \text{ MHz}, \text{Open drain}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C _{iss}		11200		pF	V _{GS} =0 V, V _{DS} =25 V, f=100 kHz
Output capacitance	C _{oss}		4880		pF	
Reverse transfer capacitance	C _{rss}		221		pF	
Turn-on delay time	t _{d(on)}		31		ns	V _{GS} =10 V, V _{DS} =50 V, R _G =2 Ω, I _D =25 A
Rise time	t _r		26		ns	
Turn-off delay time	t _{d(off)}		75		ns	
Fall time	t _f		28		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q _g		144		nC	V _{GS} =10 V, V _{DS} =50 V, I _D =25 A
Gate-source charge	Q _{gs}		40		nC	
Gate-drain charge	Q _{gd}		22		nC	
Gate plateau voltage	V _{plateau}		3.8		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V _{SD}			1.3	V	I _s =30 A, V _{GS} =0 V
Reverse recovery time	t _{rr}		123		ns	
Reverse recovery charge	Q _{rr}		223		nC	
Peak reverse recovery current	I _{rrm}		3.2		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) V_{DD}=50V, V_{GS}=10 V, L=0.3 mH, starting T_j=25 °C.

Electrical Characteristics Diagrams

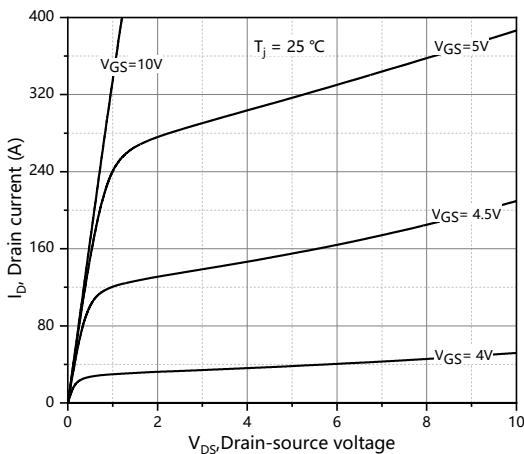


Figure 1. Typ. output characteristics

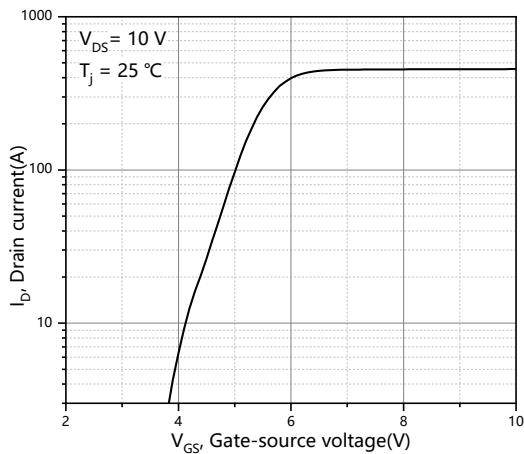


Figure 2. Typ. transfer characteristics

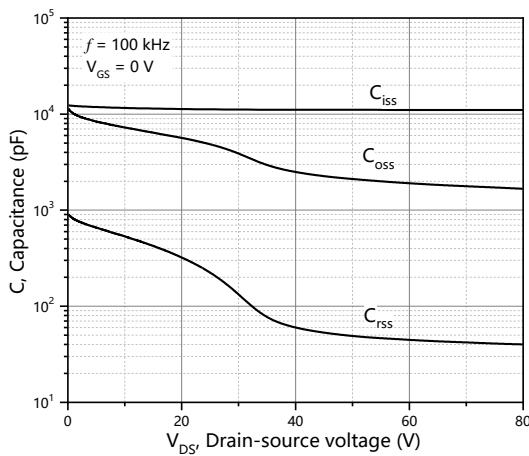


Figure 3. Typ. capacitances

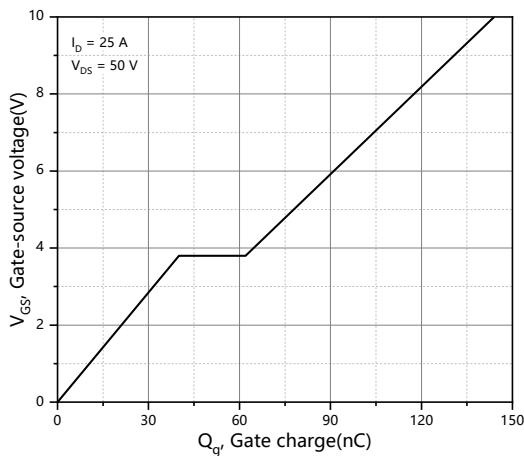


Figure 4. Typ. gate charge

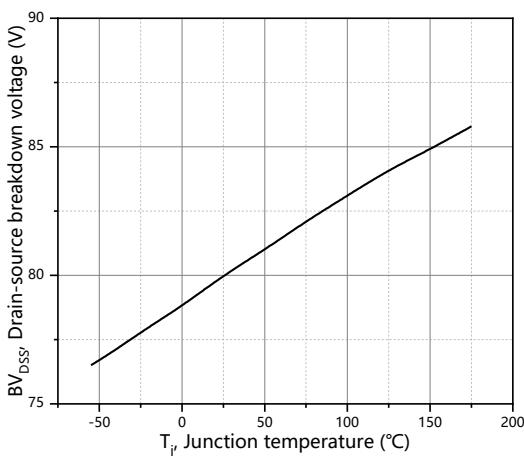


Figure 5. Drain-source breakdown voltage

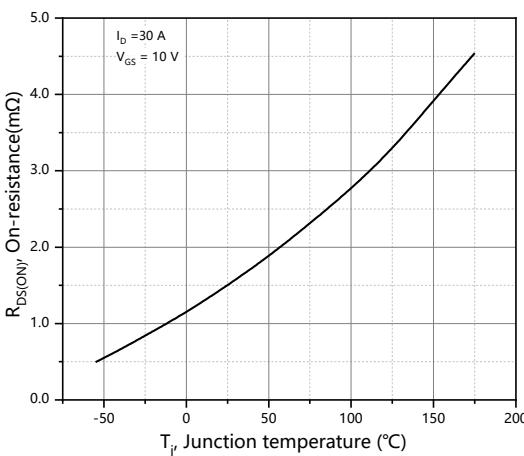
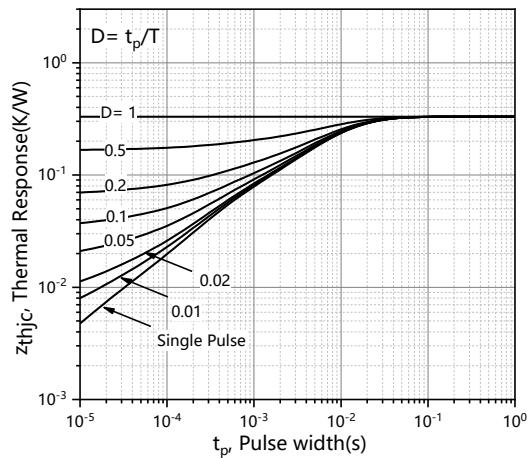
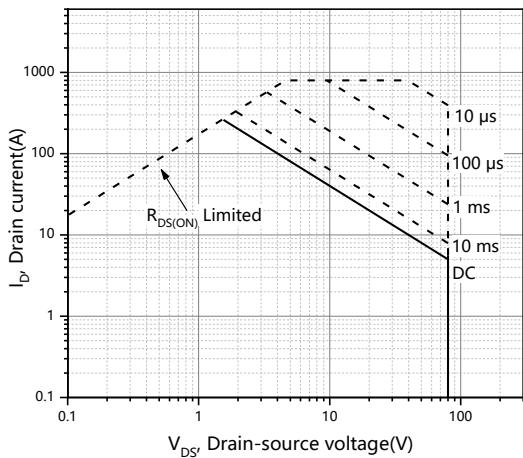
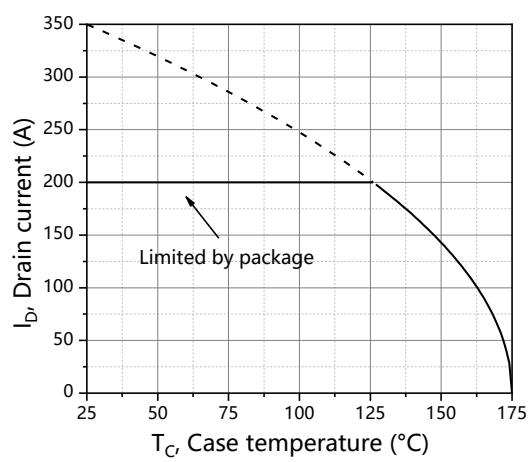
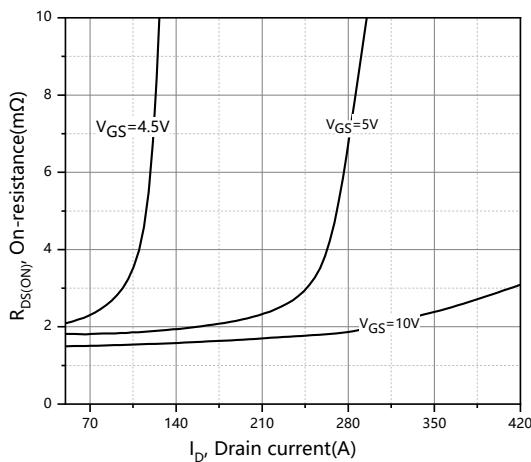
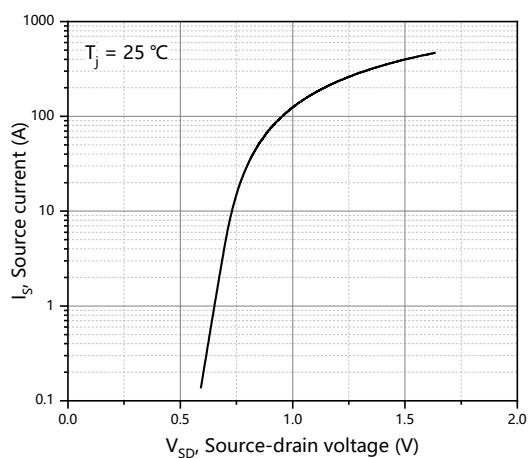
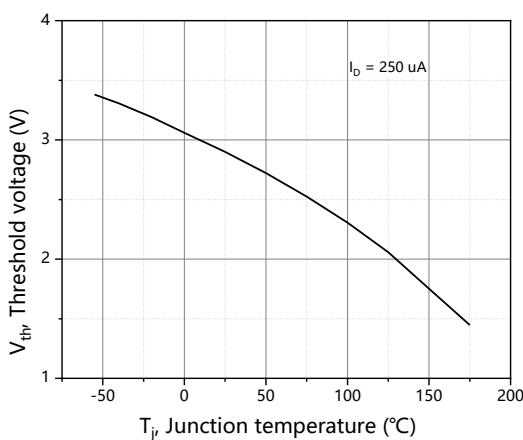


Figure 6. Drain-source on-state resistance



Test circuits and waveforms

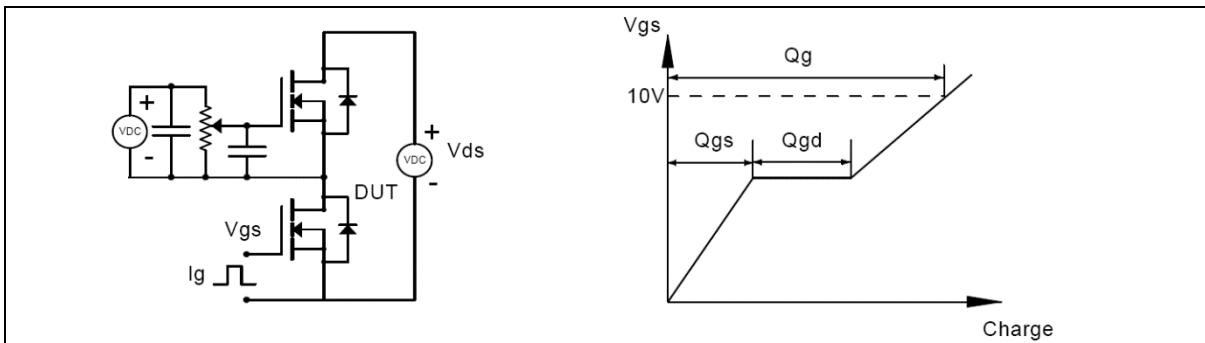


Figure 1. Gate charge test circuit & waveform

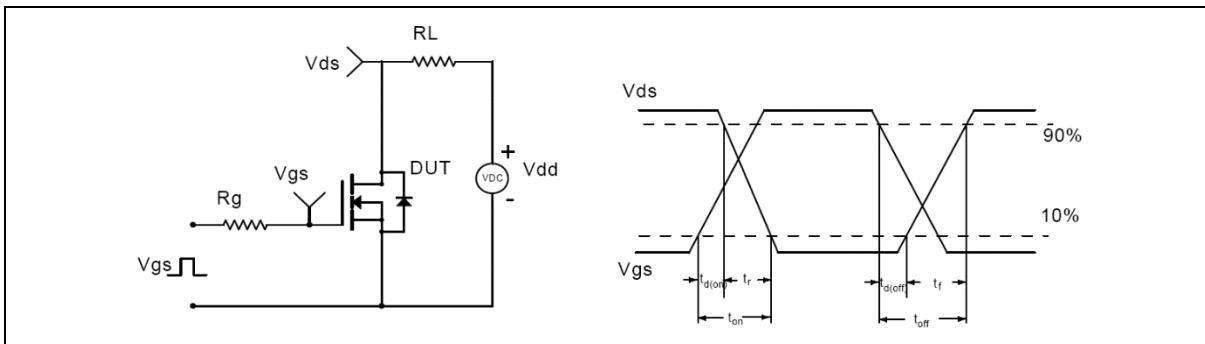


Figure 2. Switching time test circuit & waveforms

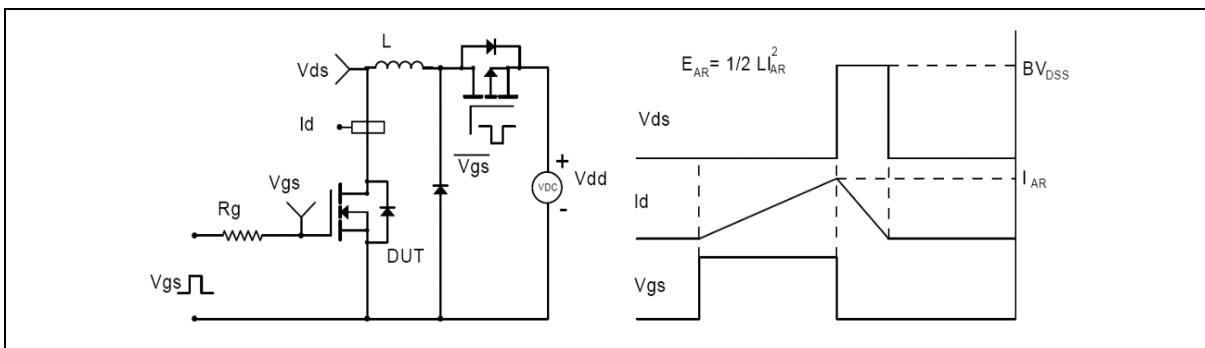


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

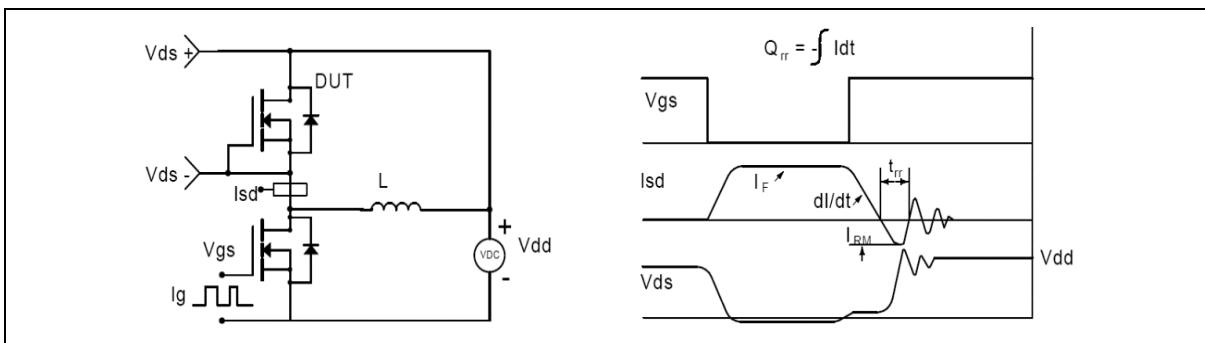
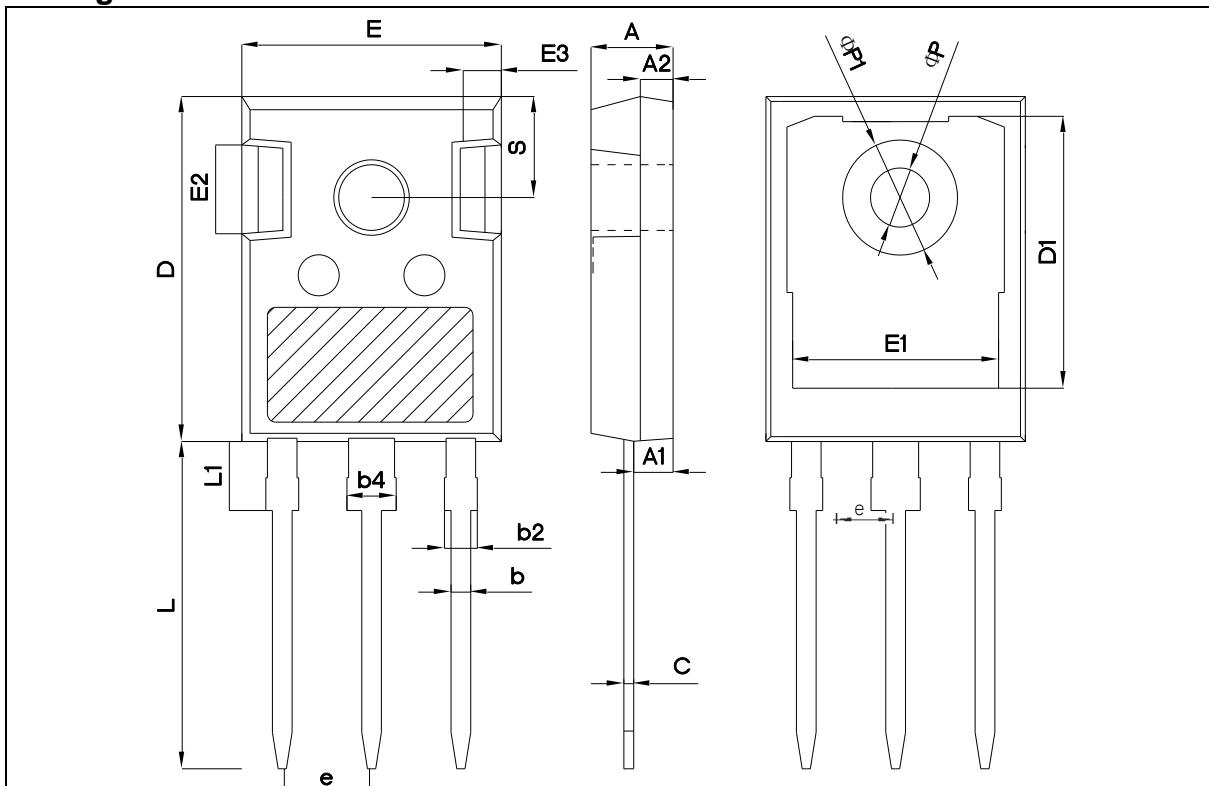


Figure 4. Diode reverse recovery test circuit & waveforms

Package Information



Symbol	mm		
	Min	Nom	Max
A	4.80	5.00	5.20
A1	2.21	2.41	2.59
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b2	1.91	2.01	2.21
b4	2.91	3.01	3.21
c	0.51	0.61	0.75
D	20.80	21.00	21.30
D1	16.25	16.55	16.85
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.80	5.00	5.20
E3	2.30	2.50	2.70
e	5.44 BSC		
L	19.82	19.92	20.22
L1	-	-	4.30
ΦP	3.40	3.60	3.80
ΦP1	-	-	7.30
S	6.15 BSC		

Version 1: TO247-P package outline dimension

Ordering Information

Package Type	Units/Reel	Reels / Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO247-P	30	11	330	6	1980

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFS08R019HNF	TO247	yes	yes	yes

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