

## General Description

FSMOS® MOSFET is based on Oriental Semiconductor's unique device design to achieve low  $R_{DS(ON)}$ , low gate charge, fast switching and excellent avalanche characteristics. The low  $V_{th}$  series is specially optimized for synchronous rectification systems with low driving voltage.

## Features

- Low  $R_{DS(ON)}$  & FOM
- Extremely low switching loss
- Excellent reliability and uniformity
- Fast switching and soft recovery



## Applications

- PD charger
- Motor driver
- Switching voltage regulator
- DC-DC convertor
- Switching mode power supply

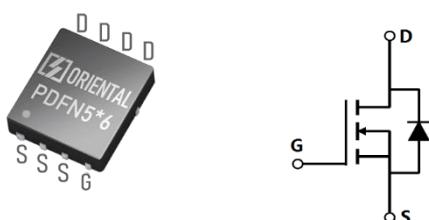
## Key Performance Parameters

Parameter	Value	Unit
$V_{DS}$	25	V
$I_D$ , pulse	800	A
$R_{DS(ON)}$ , max @ $V_{GS}=10V$	1	mΩ
$Q_g$	89	nC

## Marking Information

Product Name	Package	Marking
SFSE2S008UGF	PDFN5x6	SFSE2S008UG

## Package & Pin information



**Absolute Maximum Ratings** at  $T_j=25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	25	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current <sup>1)</sup> , $T_C=25^\circ\text{C}$	$I_D$	200	A
Pulsed drain current <sup>2)</sup> , $T_C=25^\circ\text{C}$	$I_{D,\text{pulse}}$	800	A
Continuous diode forward current <sup>1)</sup> , $T_C=25^\circ\text{C}$	$I_S$	200	A
Diode pulsed current <sup>2)</sup> , $T_C=25^\circ\text{C}$	$I_{S,\text{pulse}}$	800	A
Power dissipation <sup>3)</sup> , $T_C=25^\circ\text{C}$	$P_D$	120	W
Single pulsed avalanche energy <sup>5)</sup>	$E_{AS}$	175	mJ
Operation and storage temperature	$T_{stg}, T_j$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	1.25	$^\circ\text{C}/\text{W}$
Thermal resistance, junction-ambient <sup>4)</sup>	$R_{\theta JA}$	62	$^\circ\text{C}/\text{W}$

**Electrical Characteristics** at  $T_j=25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	$BV_{DSS}$	25			V	$V_{GS}=0 \text{ V}, I_D=250 \mu\text{A}$
Gate threshold voltage	$V_{GS(\text{th})}$	1		2.5	V	$V_{DS}=V_{GS}, I_D=250 \mu\text{A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		0.82	1	$\text{m}\Omega$	$V_{GS}=10 \text{ V}, I_D=20 \text{ A}$
Gate-source leakage current	$I_{GSS}$			100	nA	$V_{GS}=20 \text{ V}$
				-100		$V_{GS}=-20 \text{ V}$
Drain-source leakage current	$I_{DSS}$			1	$\mu\text{A}$	$V_{DS}=25 \text{ V}, V_{GS}=0 \text{ V}$
Gate resistance	$R_G$		1.4		$\Omega$	$f=1 \text{ MHz}, \text{Open drain}$

### Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C <sub>iss</sub>		4860		pF	V <sub>GS</sub> =0 V, V <sub>DS</sub> =25 V, f=100 kHz
Output capacitance	C <sub>oss</sub>		1560		pF	
Reverse transfer capacitance	C <sub>rss</sub>		72		pF	
Turn-on delay time	t <sub>d(on)</sub>		14		ns	V <sub>GS</sub> =10 V, V <sub>DS</sub> =20 V, R <sub>G</sub> =2 Ω, I <sub>D</sub> =20 A
Rise time	t <sub>r</sub>		16		ns	
Turn-off delay time	t <sub>d(off)</sub>		46		ns	
Fall time	t <sub>f</sub>		22		ns	

### Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q <sub>g</sub>		89		nC	V <sub>GS</sub> =10 V, V <sub>DS</sub> =20 V, I <sub>D</sub> =20 A
Gate-source charge	Q <sub>gs</sub>		12		nC	
Gate-drain charge	Q <sub>gd</sub>		23		nC	
Gate plateau voltage	V <sub>plateau</sub>		2.5		V	

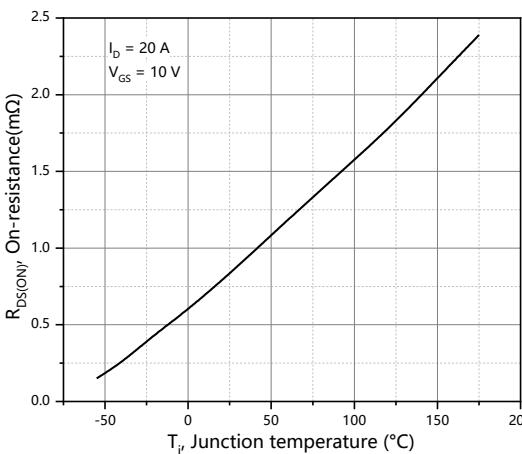
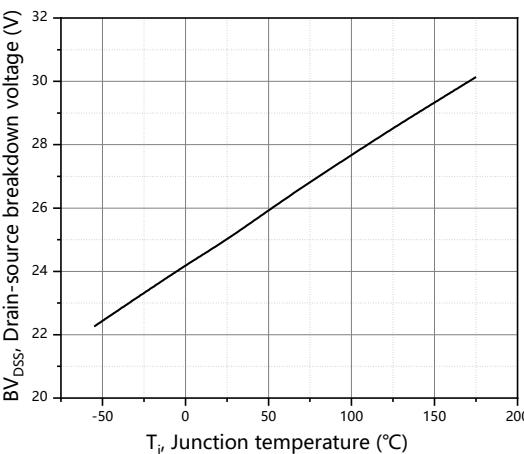
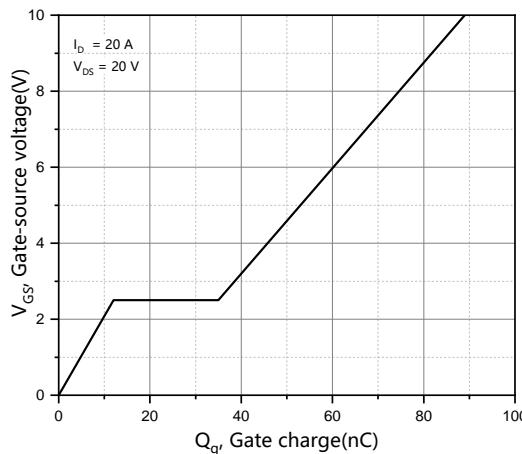
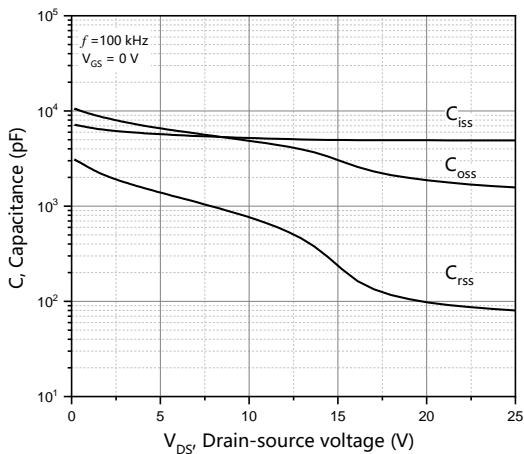
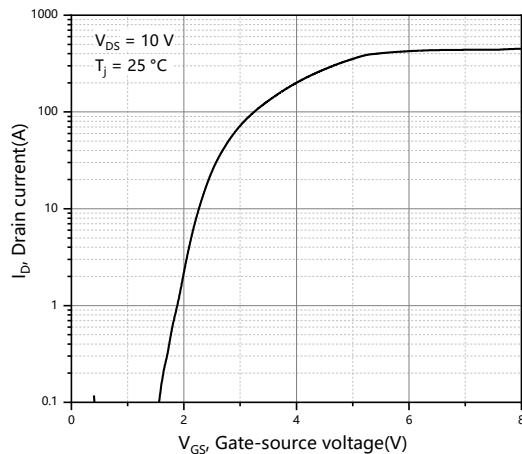
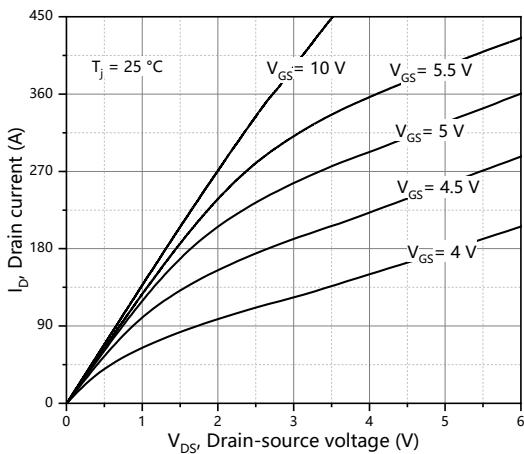
### Body Diode Characteristics

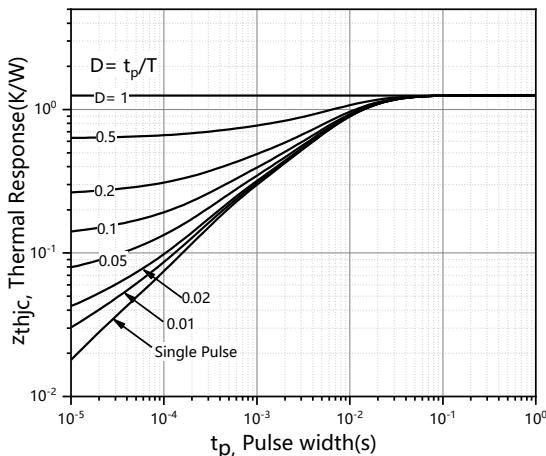
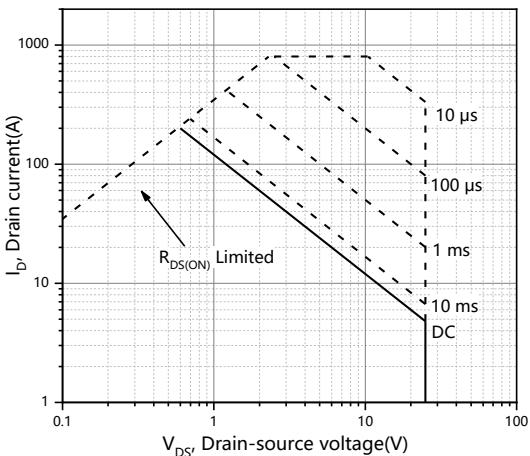
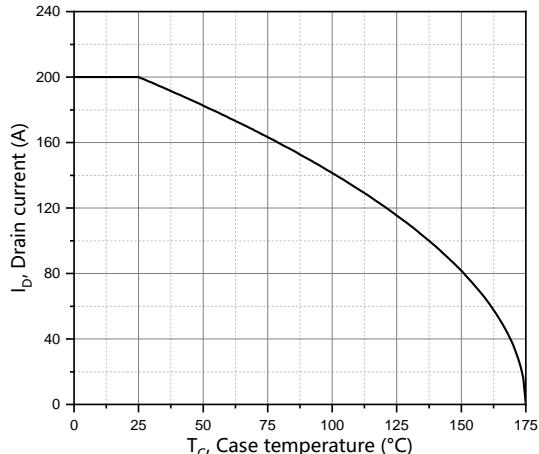
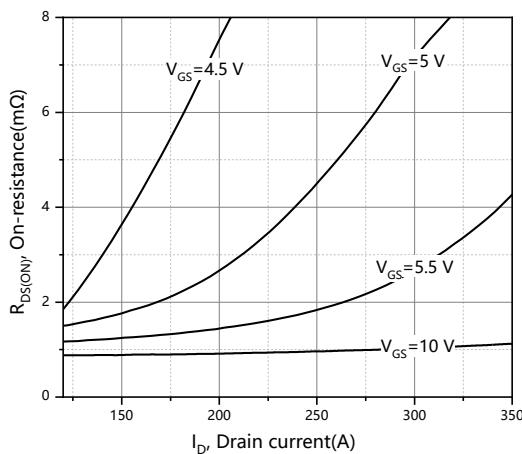
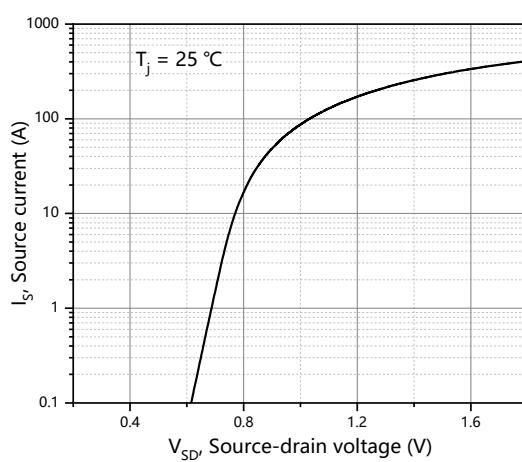
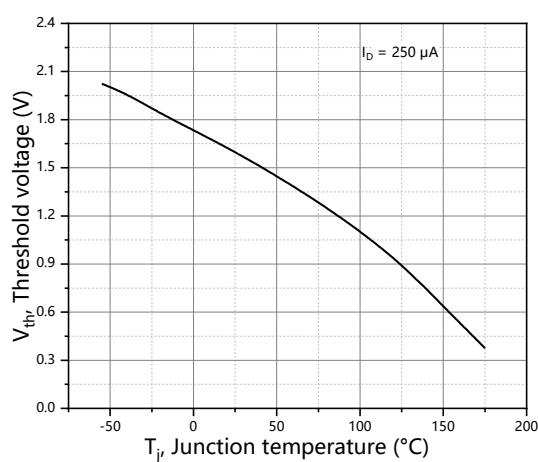
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward voltage	V <sub>SD</sub>			1.3	V	I <sub>s</sub> =20 A, V <sub>GS</sub> =0 V
Reverse recovery time	t <sub>rr</sub>		104		ns	V <sub>R</sub> =20V, I <sub>s</sub> =20A, di/dt=100 A/μs
Reverse recovery charge	Q <sub>rr</sub>		192		nC	
Peak reverse recovery current	I <sub>rrm</sub>		3.1		A	

### Note

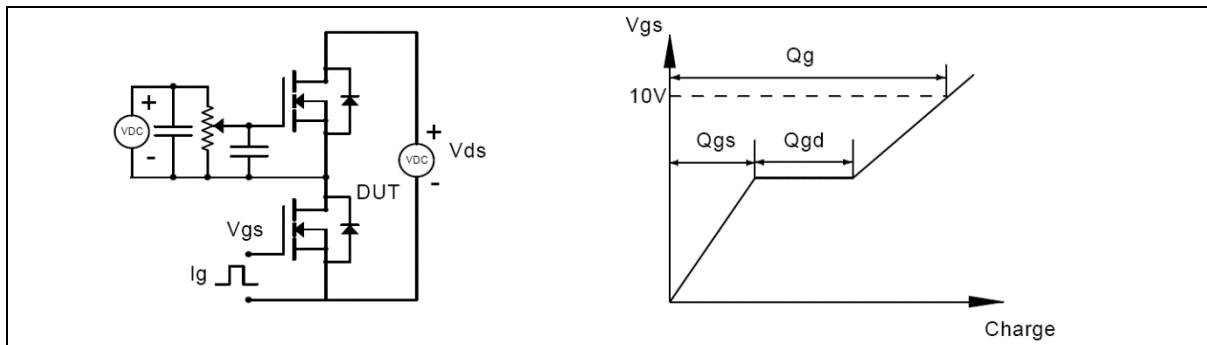
- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>a</sub>=25 °C.
- 5) V<sub>DD</sub>=50 V, V<sub>GS</sub>=10 V, L=0.3 mH, starting T<sub>j</sub>=25 °C.

## Electrical Characteristics Diagrams

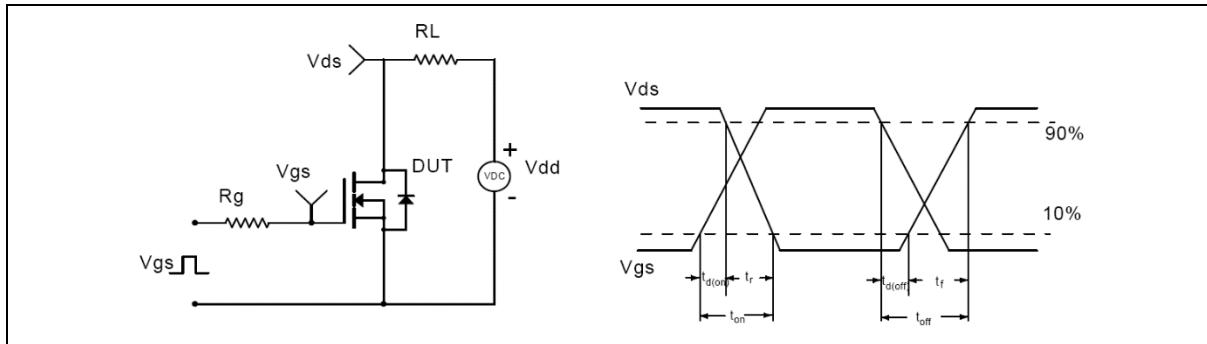




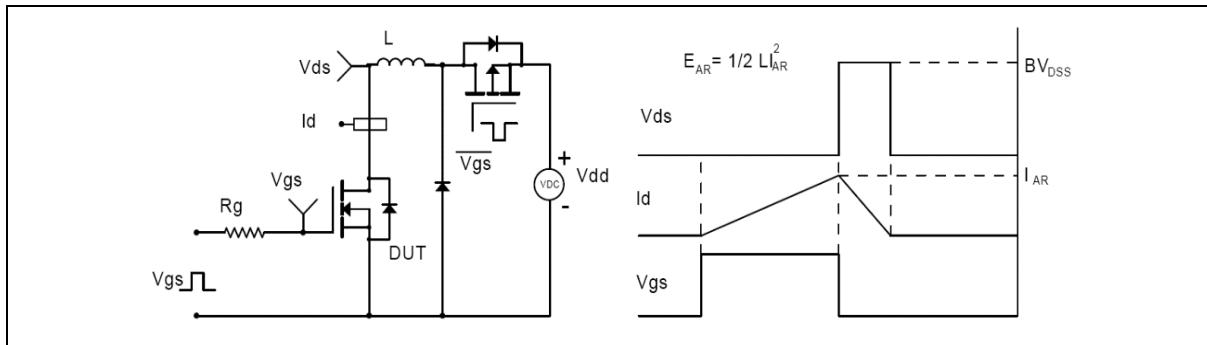
### Test circuits and waveforms



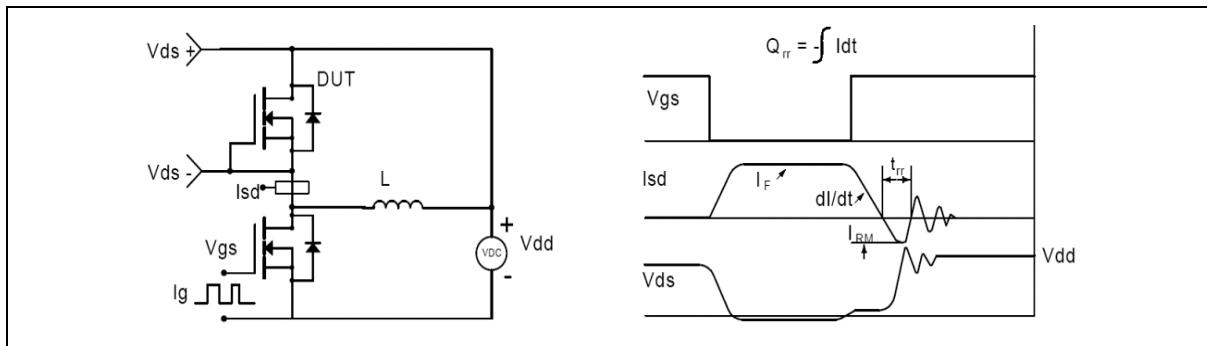
**Figure 1. Gate charge test circuit & waveform**



**Figure 2. Switching time test circuit & waveforms**

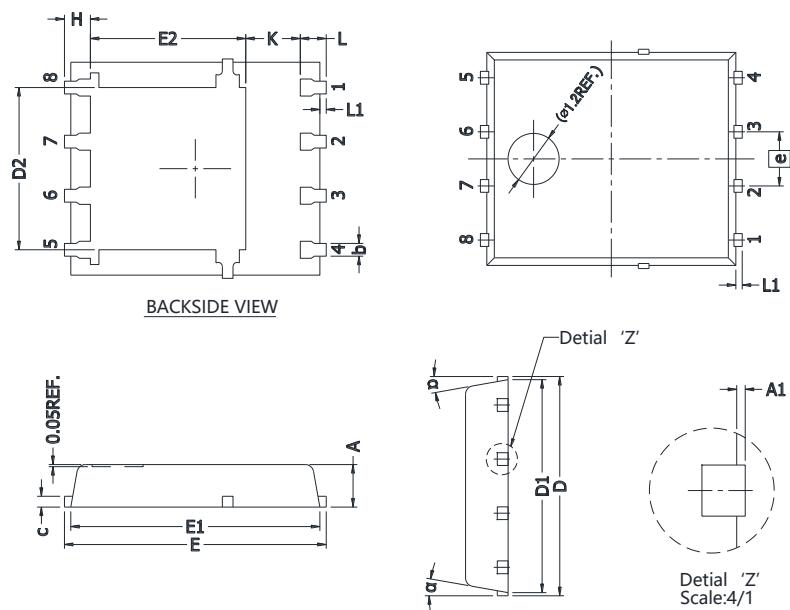


**Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms**



**Figure 4. Diode reverse recovery test circuit & waveforms**

## Package Information



Symbol	mm		
	Min	Nom	Max
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.30	0.40	0.50
c	0.20	0.25	0.30
D	5.15 BSC		
D1	5.00 BSC		
D2	3.76	3.81	3.86
E	6.15 BSC		
E1	5.80	5.85	5.90
E2	3.45	3.65	3.85
e	1.27 BSC		
H	0.51	0.61	0.71
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.08	0.15	0.23
$\alpha$	$10^\circ$	$11^\circ$	$12^\circ$

Version 1: PDFN5x6-J package outline dimension

## Ordering Information

Package Type	Units/Reel	Reels/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
PDFN5x6-J	5000	1	5000	5	25000

## Product Information

Product	Package	Pb Free	RoHS	Halogen Free
SFSE2S008UGF	PDFN5x6	yes	yes	yes

## Legal Disclaimer

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