2.69 inch AMOLED Display Series

GDOJ0269C01-T

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**2.69" AMOLED DISPLAY**
Model Name	**GDOJ0269C01-T**
Date	**2023 / 04 / 14**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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Content

1. General Description

1.1 Introduction

2.69” MDS is a color active matrix AMOLED module using Low Temperature Poly-silicon TFT’s (Thin Film Transistors) as active switching devices. This module has a 2.69inch diagonally measured active area with 800RGBx600 resolutions (800horizontal by 600vertical pixel arrays). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

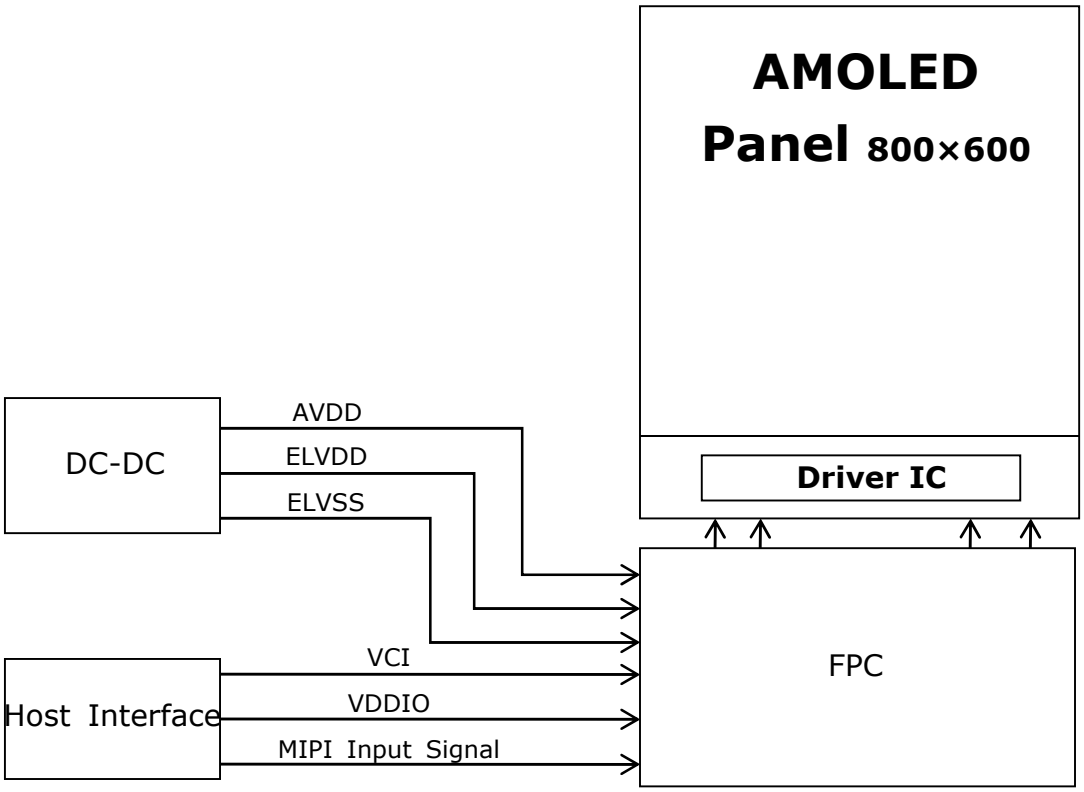


Figure 1.1

1.2 Driver IC Block Diagram

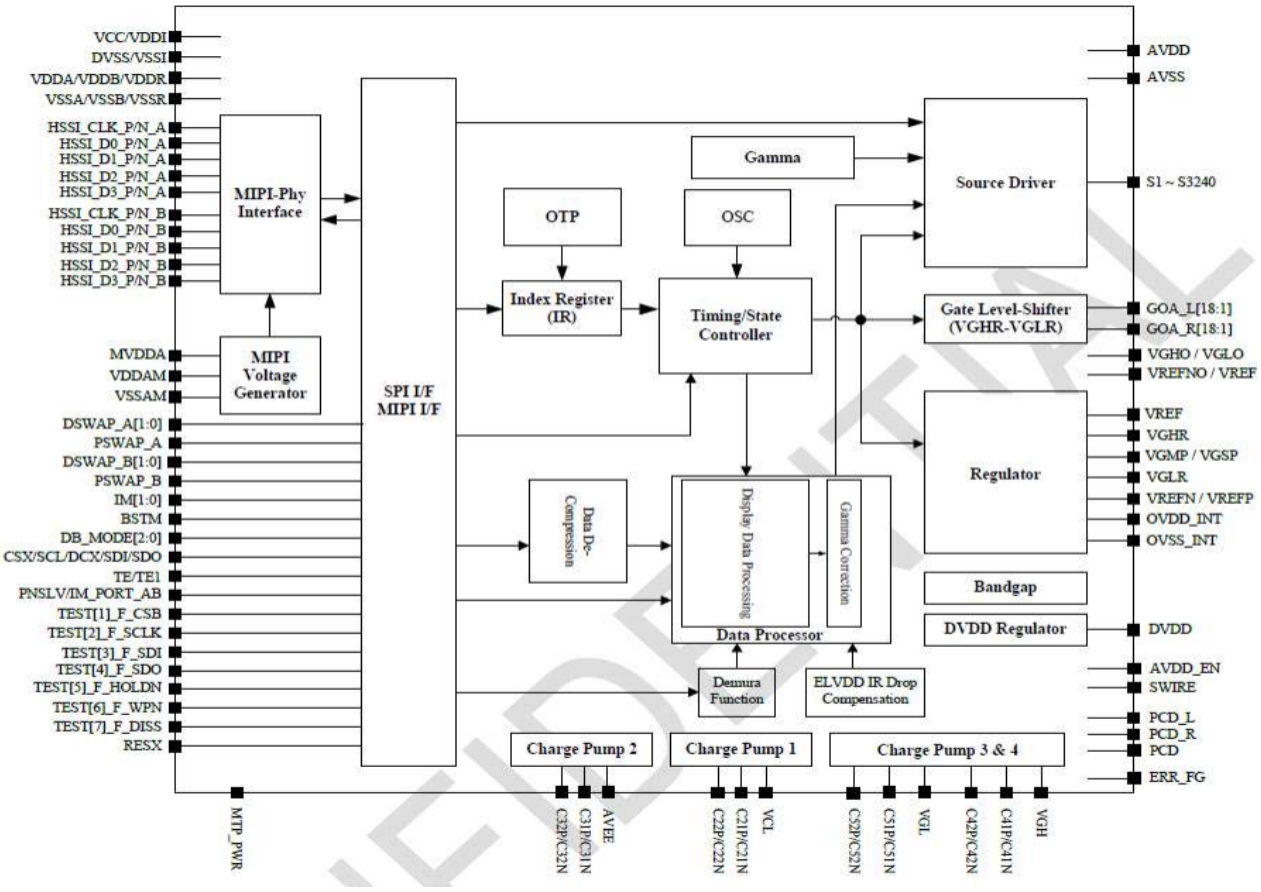


Figure 1.2

1.3 Features

1) Display Colors : 16.7M

2) Display Format : 2.69” Pentile RGB : 800×600

3) Interface : DSI 2-lane

4) Driver IC : RM69700 (Raydium)

5) Touch IC : S3601(Synaptics)

6) Polarizer : Hard Coating Polarizer

1.4 Application

- Night-vision Device

2. Mechanical Specification

Table 2.1

Item	Specifications	Unit	Remark
Panel outline	56.6(W) × 47.25(H)×0.505(T)	mm	
Number of dots	1600(W) × Pentile × 600(H)	Dots	
Active area	54.6(W) × 40.95(H)	mm	
Diagonal Inch	2.69	inch	
Pixel pitch	68.25(W) × 68.25(H)	um	
Pixel Arrangement	Pentile		
Weight	4.87±0.1	g	
Glass Thickness	0.20 (LTPS glass without PF) 0.305 (Encap)	mm	

3. Absolute Maximum Ratings

Table 3.1

Item	Symbol	Min.	Max.	Unit	Note
I/O Voltage	VDDIO	-	6.6	V	
Operation Voltage	VCI	-	6.6	V	
EL Driving Voltage	ELVDD	4.6	-	V	
	ELVSS	-3	-	V	
Supply voltage (TSP)	TSP_VDD	-0.3	3.6	V	
	IOVDD	-0.3	3.6	V	
Operating temperature	Topr	-40	85	℃	-
Storage temperature	Tstg	-55	125	℃	-

4. Electrical Characteristics

Test Condition: Temp=25±2℃

Table 4.1

Item	Min.	Typ.	Max.	Unit	Remark
Logic Power	1.62	1.8	1.98	V	
ELVDD	4.6	4.6	4.6	V	
ELVSS	-3	-2.0	-1.4	V	100mV Step
AVDD	6.8	6.8	7.8	V	
VCI	2.7	3.0	3.6	V	
VDDIO	1.62	1.8	1.98	V	
Logic Current	20	23	26	mA	
Freq	-	50	-	Hz	
VGH	5.7	6	7	V	
VGL	-7	-6	-5.4	V	

Notes :

1. VGH is TFT Gate operating voltage.
2. VGL is TFT Gate operating voltage.
3. The value is just the reference value. The customer can optimize the setting value by the different D-IC.
4. RM69700, DualRam.

5. Electro-optical Characteristics

The test of optical specifications shall be measured in a dark room (ambient luminance ≤1lux and temperature = 25±2℃) with the equipment of Luminance meter. We refer to θ, Ø=0º (=θ3) as the 3 o'clock direction (the "right"), θ, Ø=90º (= θ12) as the 12 o'clock direction ("upward"), θ, Ø=180º (= θ9) as the 9 o'clock direction ("left") and θ, Ø=270º (= θ6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay.

Table 5.1

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	Horizontal	θ_3	CR ratio≥1600	80	-	-	°	Note1
		θ_9						
	Vertical	θ_6						
		θ_{12}						
Brightness			θ=0° At Center	380	420	460	nit	
Contrast ratio		CR	θ=0°	100,000:1	-	-	-	Note2
Brightness Uniformity		LRU	W255	75	80	-	%	Note3
Color of CIE coordinate	White	x_W	θ=0°	0.2790	0.2990	0.3190	CIE 1931	Note4
		y_W		0.2949	0.3149	0.3349		
	Red	x_R		0.660	0.680	0.700		
		y_R		0.300	0.320	0.340		
	Green	x_G		0.215	0.245	0.275		
		y_G		0.685	0.715	0.745		
	Blue	x_B		0.121	0.141	0.161		
		y_B		0.025	0.045	0.065		
Color Gamut			θ=0° vs. NTSC	-	100	-	%	
Response Time			G To G			2	ms	
Cross Talk(5nit)			Window: black Background: gray127	-	3.5	5	%	Note5
Cross Talk(100nit&420nit)					-	3		
Colorshift			W255	3(30°)	4(45°)	5(60°)	JNCD	
Gamma			Subsection Control	1.9	2.2	2.5	-	-
Life time	LT93 B10		Room temperature	-	240	-	hrs	
	LT93 B10		50℃		72		hrs	

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 1600:1. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the panel surface (see Figure 3).

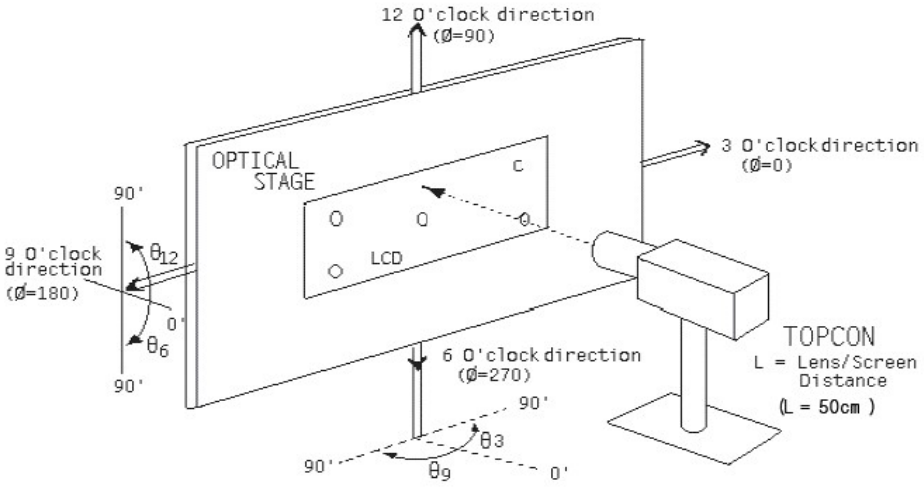


Figure 5.1

2. Contrast measurements shall be made at viewing angle of θ= 0º and at the center of the panel surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 3) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Uniformity. LRU Refer to figure as below：

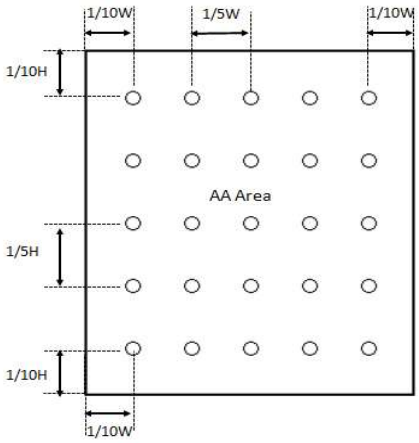


Figure 5.2

Uniformity measurements shall be made atθ=0° and at the different points of the panel surface. Luminance shall be measured with all pixels in the view field set to W/R/G/B at 255 Gary level, respectively. Luminance uniformity=Lmin/Lmax ×100%

4. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. Crosstalk measurement shall be done at the center of the different pattern and the result shall be calculated as follow formula.

a. measure luminance at the center.

b. calculate cross talk as below equation:

$$\text{Crosstalk(V)}=\left|\frac{L_{Vinf}-L_{ref}}{L_{ref}}\right|\times 100\%$$

$$\text{Crosstalk(H)}=\left|\frac{L_{hinf}-L_{ref}}{L_{ref}}\right|\times 100\%$$

Figure 5.3

6. FPC Pin Assignment

Main FPC assignment- AMOLED Panel Input/output Signal Interface. Recommended connector: Molex5052743040

Table 6.1

No.	Name	No.	Name
1	NC	2	GND
3	NC	4	ELVDD
5	NC	6	ELVDD
7	NC	8	ELVSS
9	GND	10	ELVSS
11	D1N	12	AVDD
13	D1P	14	GND
15	GND	16	VDDIO
17	CLKN	18	VCI
19	CLKP	20	GND
21	GND	22	SWIRE
23	D0N	24	OLED_EN
25	D0P	26	ERR_FG
27	GND	28	TE
29	MTP_PWR	30	RESX

7. AC Characteristics

7.1 Serial Interface Characteristics

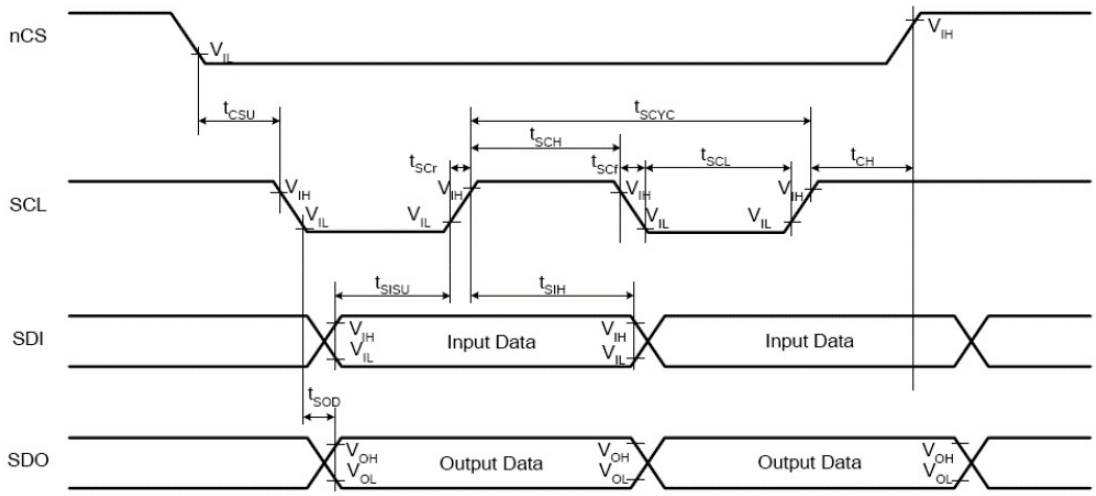


Figure 7.1

Table 7.1

Signal	Symbol	Parameter	MIN	MAX	Unit
SCL	T_{SCYC}	Clock cycle (Write)	100	-	ns
	T_{SCYC}	Clock cycle (Read)	300	-	ns
	T_{SCH}	Clock “H” pulse width (Write)	40	-	ns
	T_{SCH}	Clock “H” pulse width (Read)	140	-	ns
	T_{SCL}	Clock “L” pulse width (Write)	40	-	ns
	T_{SCL}	Clock “L” pulse width (Read)	140	-	ns
	T_{SCr}	Clock rise time	-	5	ns
	T_{SCf}	Clock fall time	-	5	ns
nCS	T_{CSU}	Chip select setup time	20	-	ns
	T_{CH}	Chip select hold time	50	-	ns
SDI	T_{SISU}	Data input setup time	20	-	ns
	T_{SIH}	Data input hold time	20	-	ns
SDO	T_{SOD}	Data output setup time	-	120	ns
	T_{SOH}	Data output hold time	5	-	ns

Notes:

1.Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

2.Ta = -40°C to 85°C, VDDI=1.62V to 1.98V, VCI=2.5V to 3.6V, GND=0V

7.2 I2C Bus Timing Characteristics

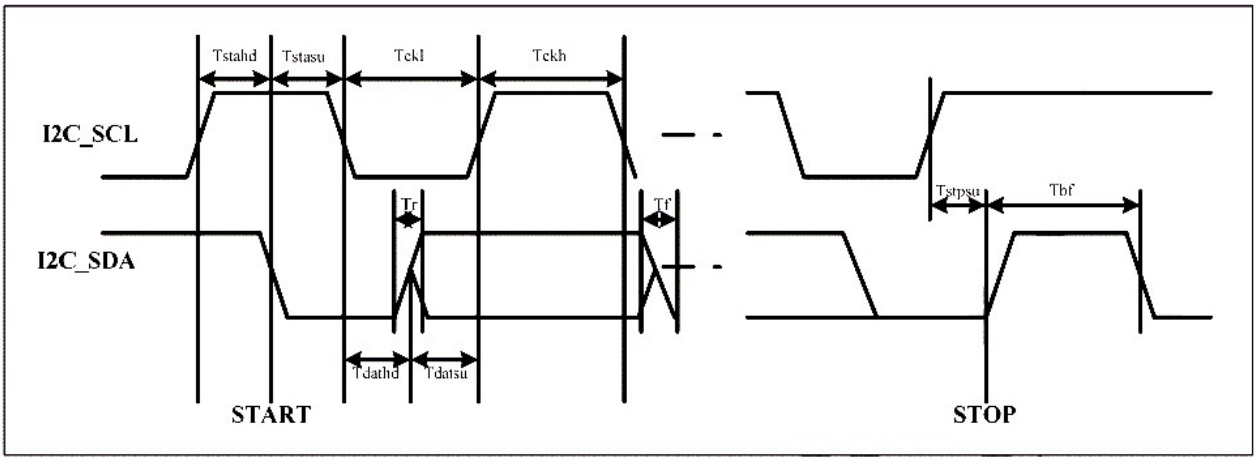


Figure7.2

Table 7.2

Signal	Symbol	Parameter	MIN	MAX	Unit
I2C_SCL	Tckl + Tckh	Operate frequency	-	400	ns
	Tckl	CLK low	1300	-	ns
	Tckh	CLK high	600	-	ns
I2C_SDA	Tr	Data rising time	-	300	ns
	Tf	Data falling time	-	300	ns
	Tdathd	Data hold time	0	900	ns
	Tdatsu	Data setup time	100	-	ns
	Tstahd	Start hold time	600	-	ns
	Tstasu	Start setup time	600	-	ns
	Tstpsu	Stop setup time	600	-	ns
	Tbf	Bus free time	1300	-	ns

Notes:

1. Logic high and low levels are specified as 20% and 80% of IOVCC for input signals.
2. Ta=-40 to 85℃, IOVCC=1.62V to 1.98V, VCI=2.5V to 3.6V, GND=0V.

7.3 RGB Interface Characteristics

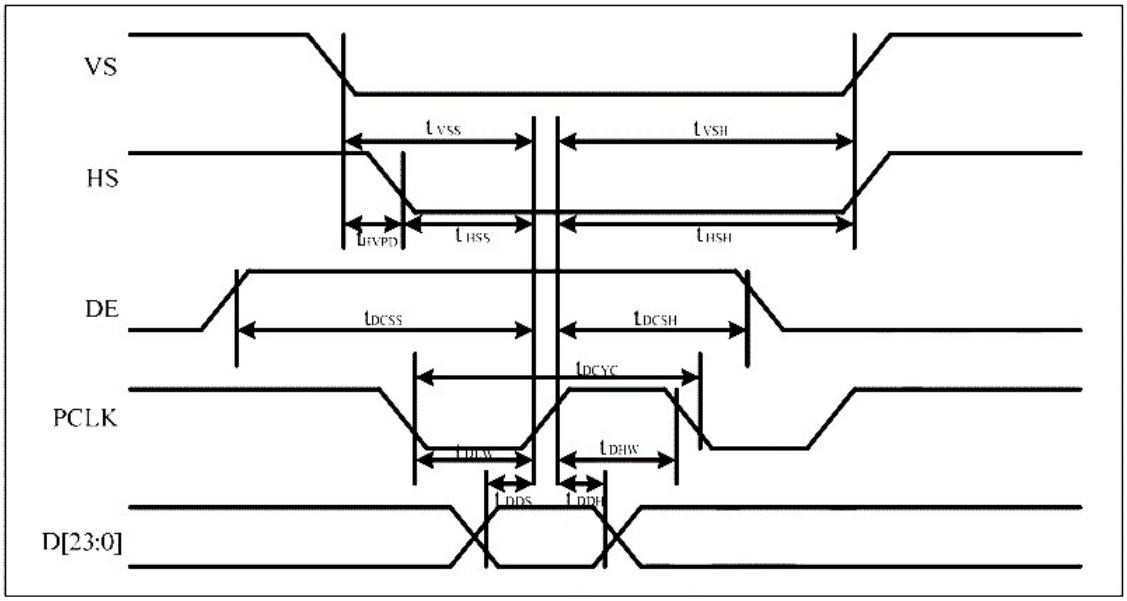


Figure 7.3

Table 7.3

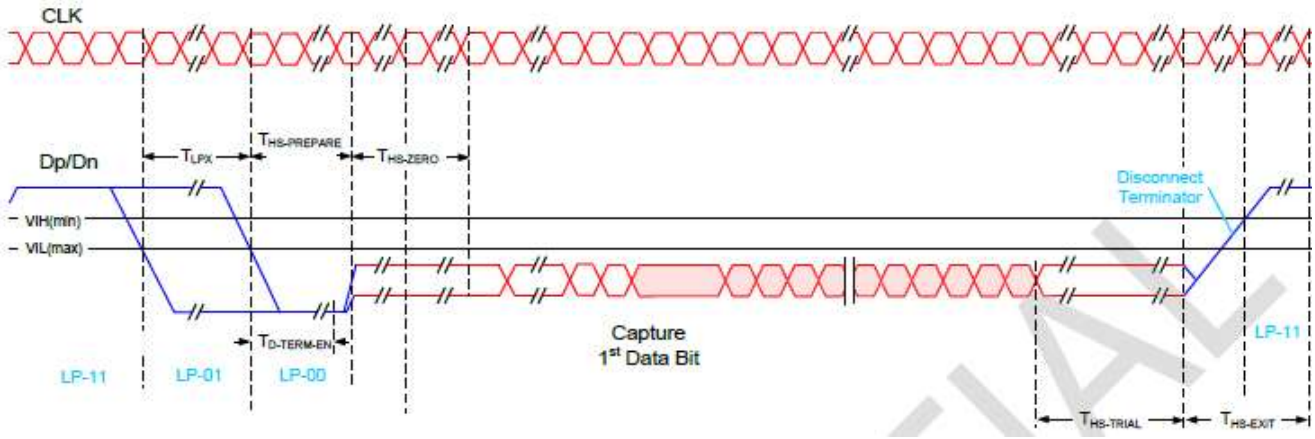
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
PCLK	t_{DCYC}	PCLK cycle time	15	-	-	ns
	t_{DLW}	PCLK low pulse width	7	-	-	ns
	t_{DHW}	PCLK high pulse width	7	-	-	ns
VS	t_{VSS}	VS setup time	3	-	-	ns
	t_{VSH}	VS hold time	3	-	-	ns
HS	t_{HSS}	HS setup time	3	-	-	ns
	t_{HSH}	HS hold time	3	-	-	ns
	t_{HVPD}	HS to VS falling edge	400	-	-	ns
DE	t_{DCSS}	DE setup time	3	-	-	ns
	t_{DCSH}	DE hold time	3	-	-	ns
D[23:0]	t_{DDS}	Data setup time	3	-	-	ns
	t_{DDH}	Data hold time	3	-	-	ns

Notes:

1. Logic high and low levels are specified as 20% and 80% of IOVCC for input signals.
2. Ta=-40 to 85℃, IOVCC=1.62V to 1.98V, VCI=2.5V to 3.6V, GND=0V.

7.4 DSI Timing Characteristics

■ HS Data Transmission Burst



■ HS clock transmission

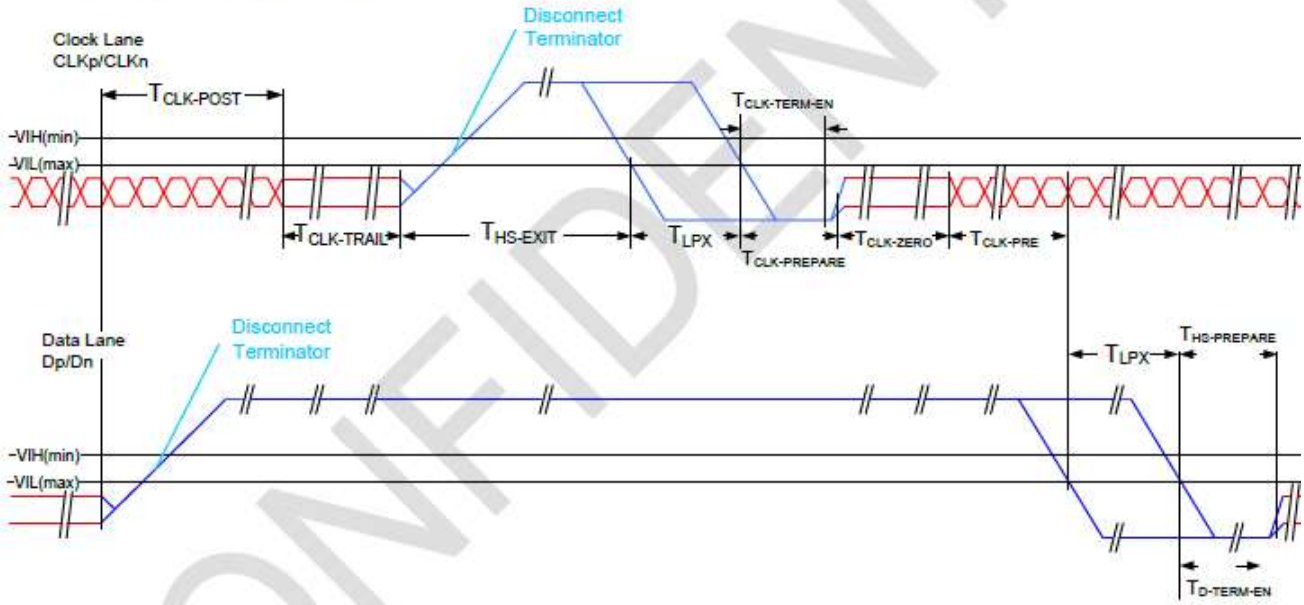


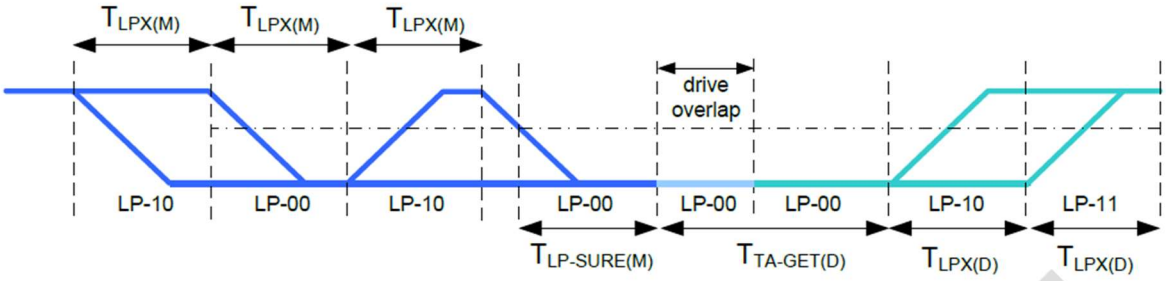
Figure 7.4

Table 7.4 Time parameter

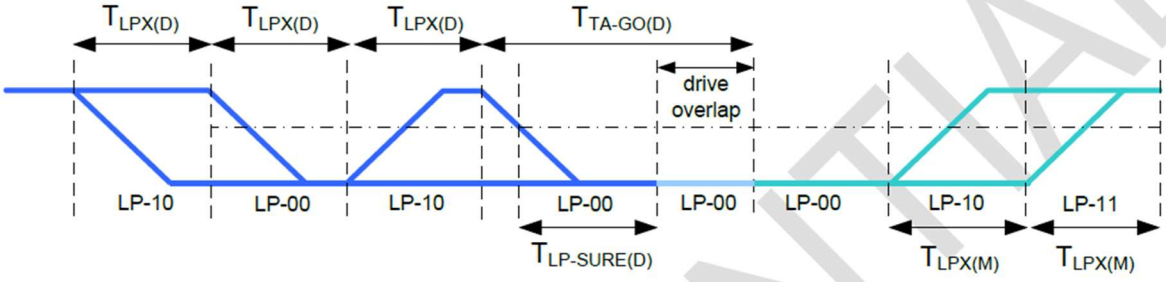
Parameter	Description	MIN	MAX	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRIAL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns+52×UI		ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300		ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS	Time for Dn to	38	ns

	line termination, Starting from the time point when Dn crosses $V_{IL, MAX}$.	reach $V_{TERM-EN}$		
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8		UI
$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time that the transmitter drives the HS-0 state prior to starting the Clock.	300		ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL, MAX}$.	Time for Dn to reach $V_{TERM-EN}$	35ns+4×UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	40ns+4×UI	85ns+6×UI	ns
$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$+ time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns+10×UI		ns
$T_{HS-TRIAL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60ns+4×UI		ns
$T_{AB-SKEW}$	Timing Skew between Port A and Port B		100	

■ Bus Turnaround Procedure (From MPU to display module)



Bus turnaround (BAT) timing



Bus turnaround (BAT) from display module to MPU timing

Figure 7.5

Table 7.5

■ Timing Specifications for Low Power Transmission:

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

Notes:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

7.5 Reset Timing

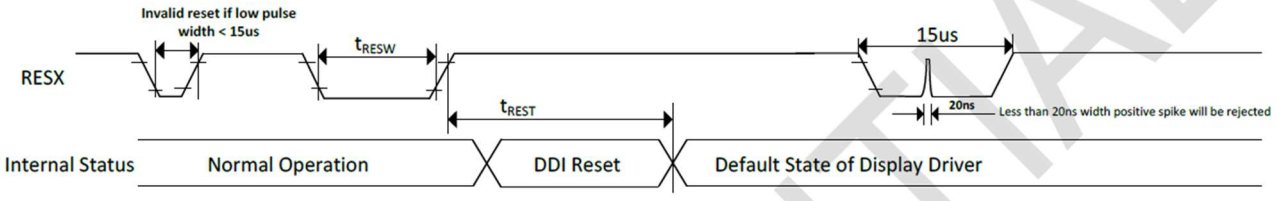


Figure 7.6

Table 7.6

Reset timing @VDDI=1.62V to 1.98V, VSSA=DVSS=VSSI=0V, Ta=-40℃ to 85℃

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	Reset low pulse width	15	-	-	1. Shorter than 5us, Reset rejected 2. Longer than 15μs, IC reset 3. Between 5μs and 15μs, It depends on voltage and temperature condition.	μs
t_{REST}	Reset complete time	-	-	10	When reset applied at sleep-in mode	ms
		-	-	120	When reset applied at sleep-out mode	ms

7.6 Touch Panel I2C Timing Characteristics

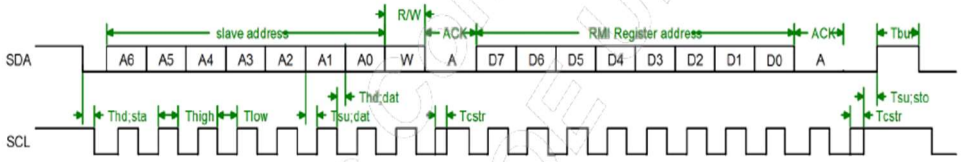


Figure 7.7

Table 7.7

Parameter	Symbol	Standard Mode			Fast Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	kHz
Clock stretch time	t_{CSTR}	-	<25	-	-	<25	-	us
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	0.6	-	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	us
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	us
Setup time for repeated START condition	$t_{SU;STA}$	4.7	-	-	0.6	-	-	us
Data hold time	$t_{HD;DAT}$	0	-	-	0	-	-	us
Data out valid time	$t_{VALID;DATO}$	-	-	3.45	-	-	0.9	us
Data setup time	$t_{SU;DAT}$	250	-	-	100	-	-	ns
Rise time of SDA/SCL	t_R	-	-	1000	$20 + 0.1C_B$	-	300	ns
Fall time of SDA/SCL	t_F	-	-	300	$20 + 0.1C_B$	-	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	-	0.6	-	-	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	us
Capacitive load for each bus line	C_B	-	-	400	-	-	400	pF

7.7 Touch Panel RESET Timing Characteristics

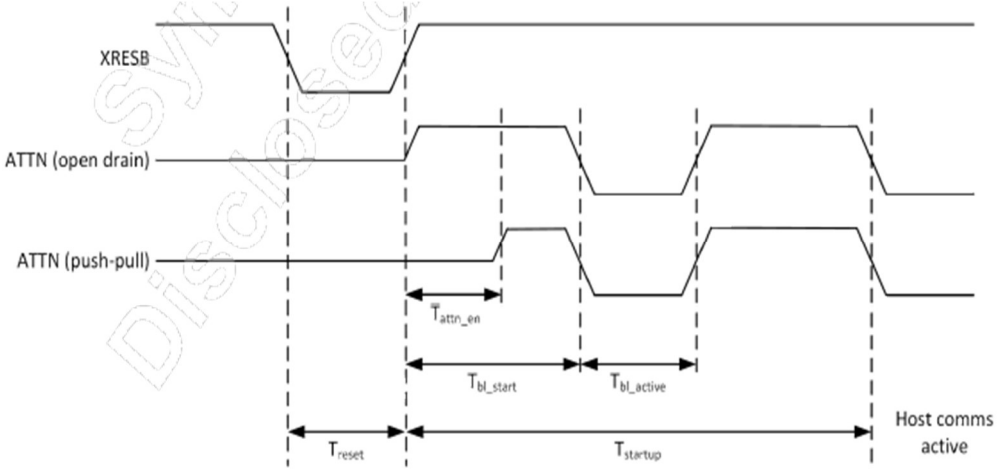


Figure 7.8

Table 7.8

Power supply	Min	Max	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	-	45	ms
$T_{startup}$	-	45	ms
T_{bl_start} (bootloader start)	-	30	ms
T_{bl_active} (bootloader active)	-	15	ms
T_{reset}	100	-	ns

8. Recommended Operating Sequence

8.1 Display Power on/off Sequence

■ Power Sequence and Generation

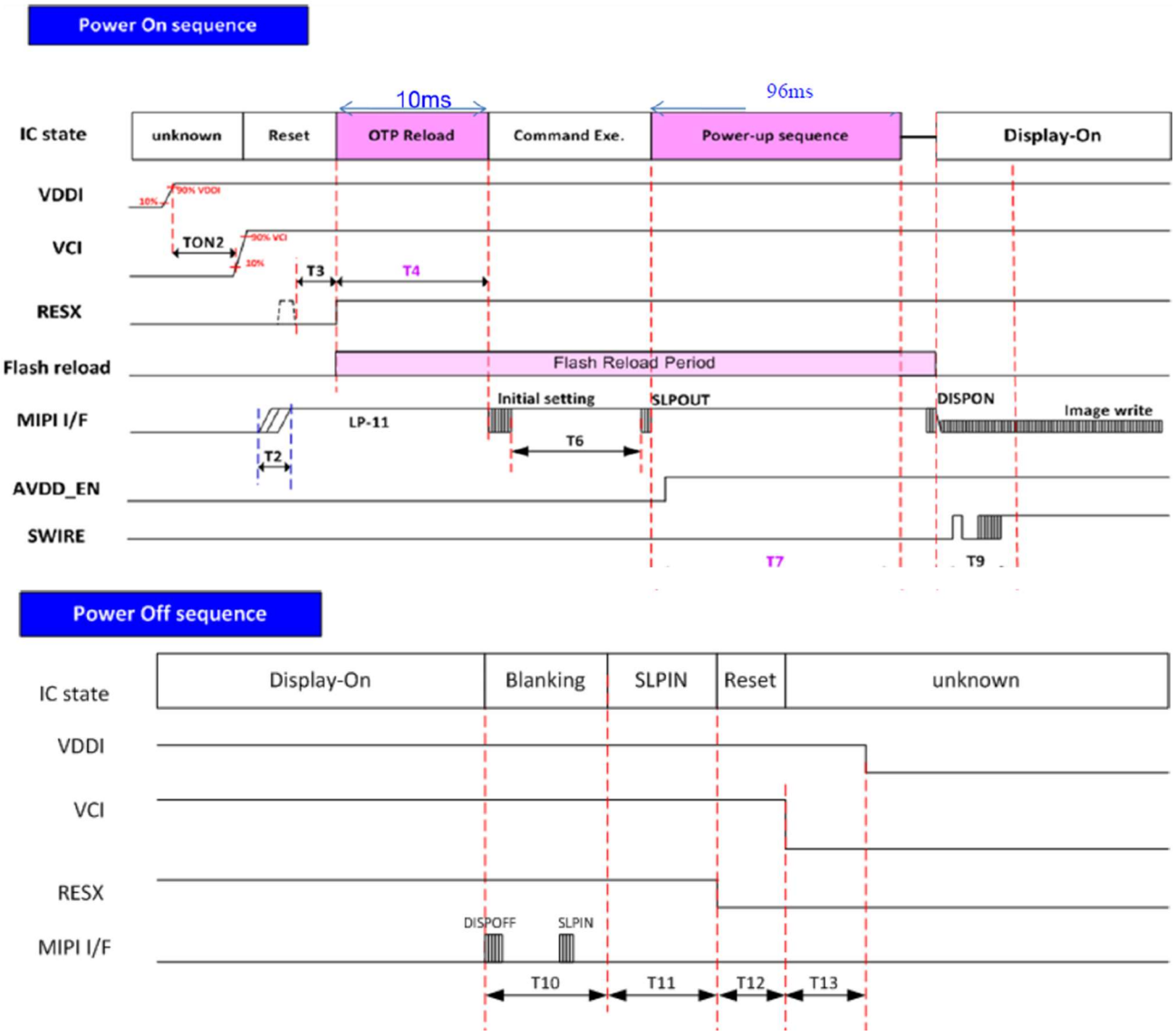


Figure 8.1

■ **Timing Specification of Power On/Off Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
TON2	2	-	-	ms	
T2	1	-	-	ms	MIPI stabilization time
T3	1	-	-	ms	Effective hardware reset period
T4	10	-	-	ms	OTP reload time
T6	0	-	-	ms	Initial code input finish to SLPOUT command input
T7	-	96	-	ms	Normal power-up sequence
T9	2	-	-	VS	Display-On Blanking region
T10	2	-	-	VS	Display-Off blanking region
T11	1	-	-	VS	Blanking region
T12	1	-	-	ms	Effective hardware reset period
T13	2	-	-	ms	Power off period

Notes:
VS means the time period of a complete display frame and is approximately 16ms if internal display timing is used.

8.2 Touch Panel Power on Sequence

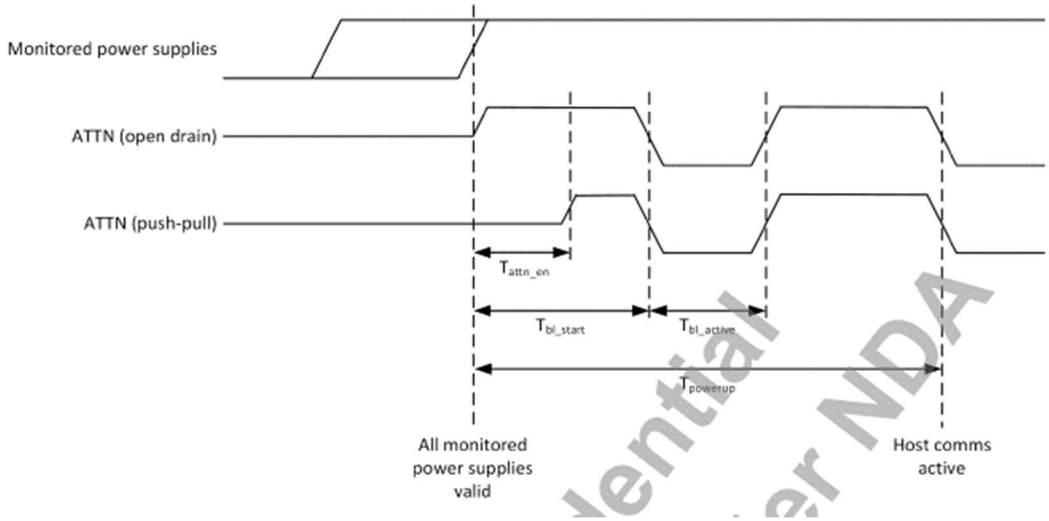


Figure 8.2

Table 8.2

Power supply	Min	Max	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	-	45	ms
$T_{startup}$	-	45	ms
T_{bl_start} (bootloader start)	-	30	ms
T_{bl_active} (bootloader active)	-	15	ms
T_{reset}	100	-	ns

9. Outline Information

9.1 Total Outline

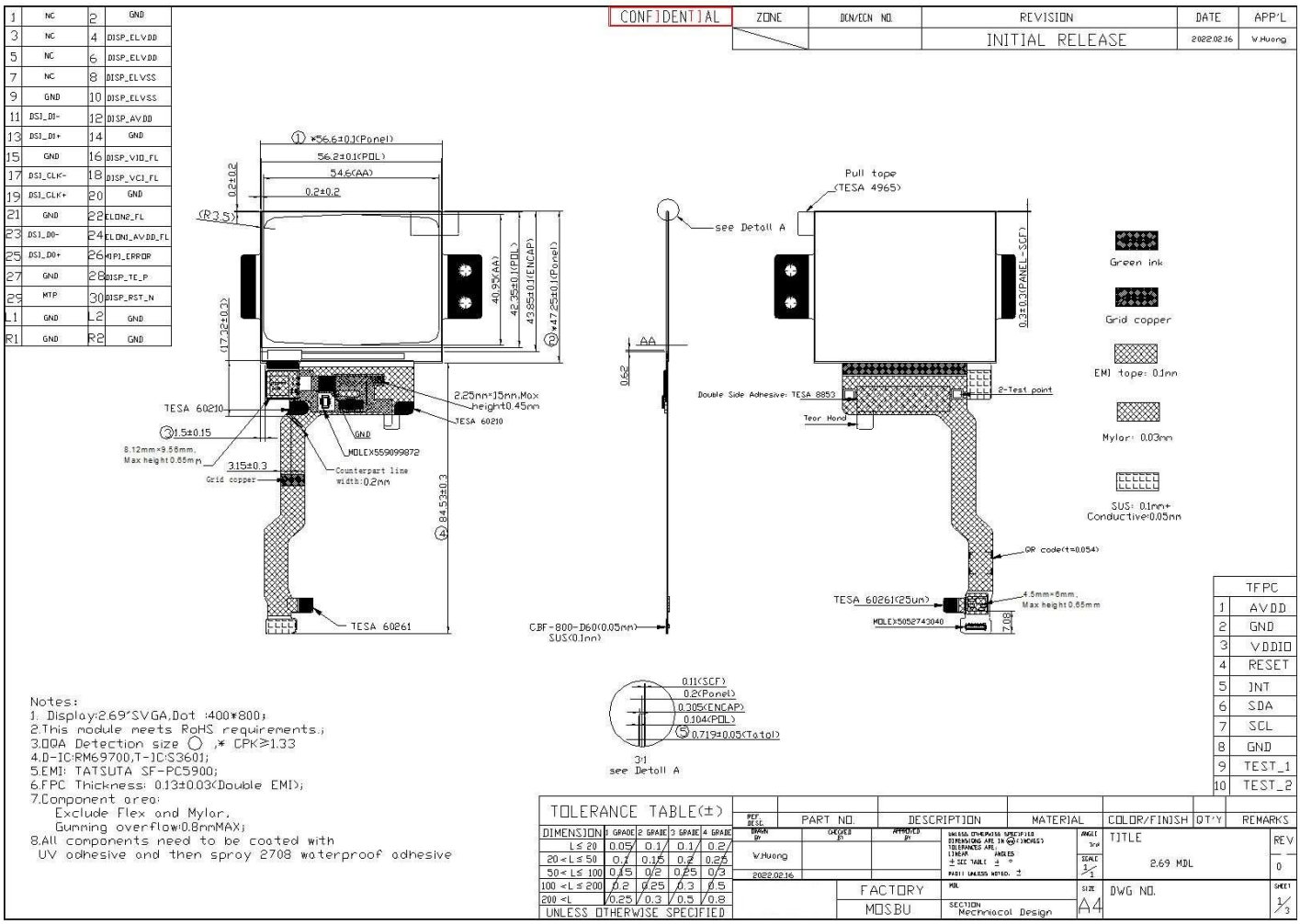


Figure 9.1

9.2 Main FPCB Drawing

9.2.1 Main FPC Schematic Diagram

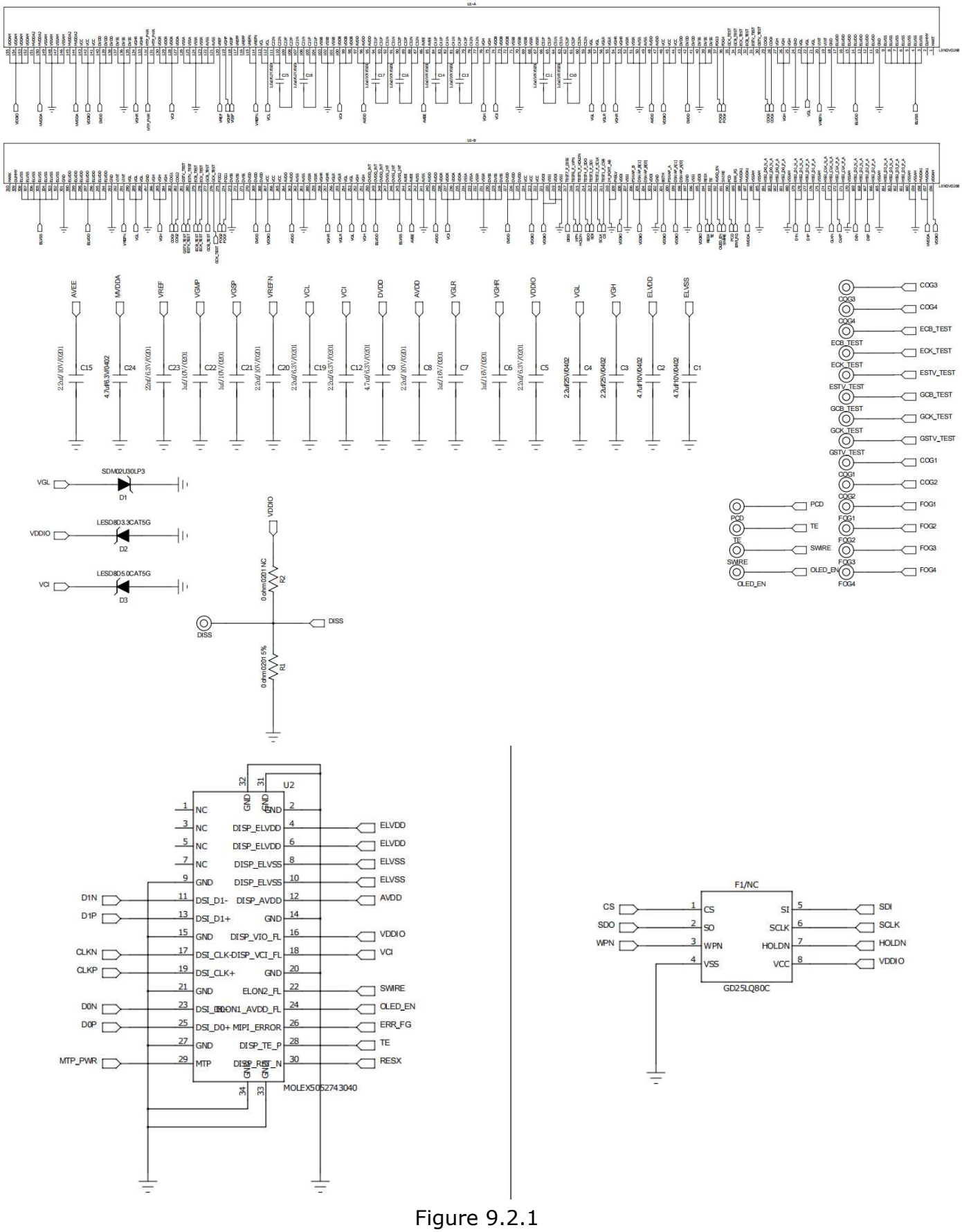


Figure 9.2.1

9.2.2 Main FPC Electronic Part List

Table 9.2

Comment	Description	Designator	Footprint	Quantity	Value
Cap	Capacitor	C16-17	0201	2	1uF/10V
Cap	Capacitor	C10-11 C13-14	0201	4	1uF/16V
Cap	Capacitor	C18,C25	0201	2	1uF/6.3V
Cap	Capacitor	C21-22	0201	2	1uF/10V
Cap	Capacitor	C6-7	0201	2	1uF/16V
Cap	Capacitor	C8,C15,C20	0201	3	2.2uF/10V
Cap	Capacitor	C5,C12,C19	0201	3	2.2uF/6.3V
Cap	Capacitor	C23	0201	1	22nF/6.3V
Cap	Capacitor	C9	0201	1	4.7uF/6.3V
Cap	Capacitor	C3-4	0402	2	2.2uF/25V
Cap	Capacitor	C1-2	0402	2	4.7uF/10V
Cap	Capacitor	C24	0402	1	4.7uF/6.3V
Diode	diode	D1	SDM02U30LP3	1	
Diode	diode	D2/NC	LESD8D5.0CT5G,LESD8D3.3CAT5G	1	NC
Diode	diode	D3/NC	LESD8D5.0CT5G,LESD8D5.0CAT5G	1	NC
Res1	Resistor	R1	0201	1	0ohm/5%
Res1	Resistor	R2/NC	0201	1	0ohm/5%
u2	Connector		MOLEX5052743040	1	
flash		F1/NC	GD25LQ80C	0	NC

9.2.3 Main FPC Placement

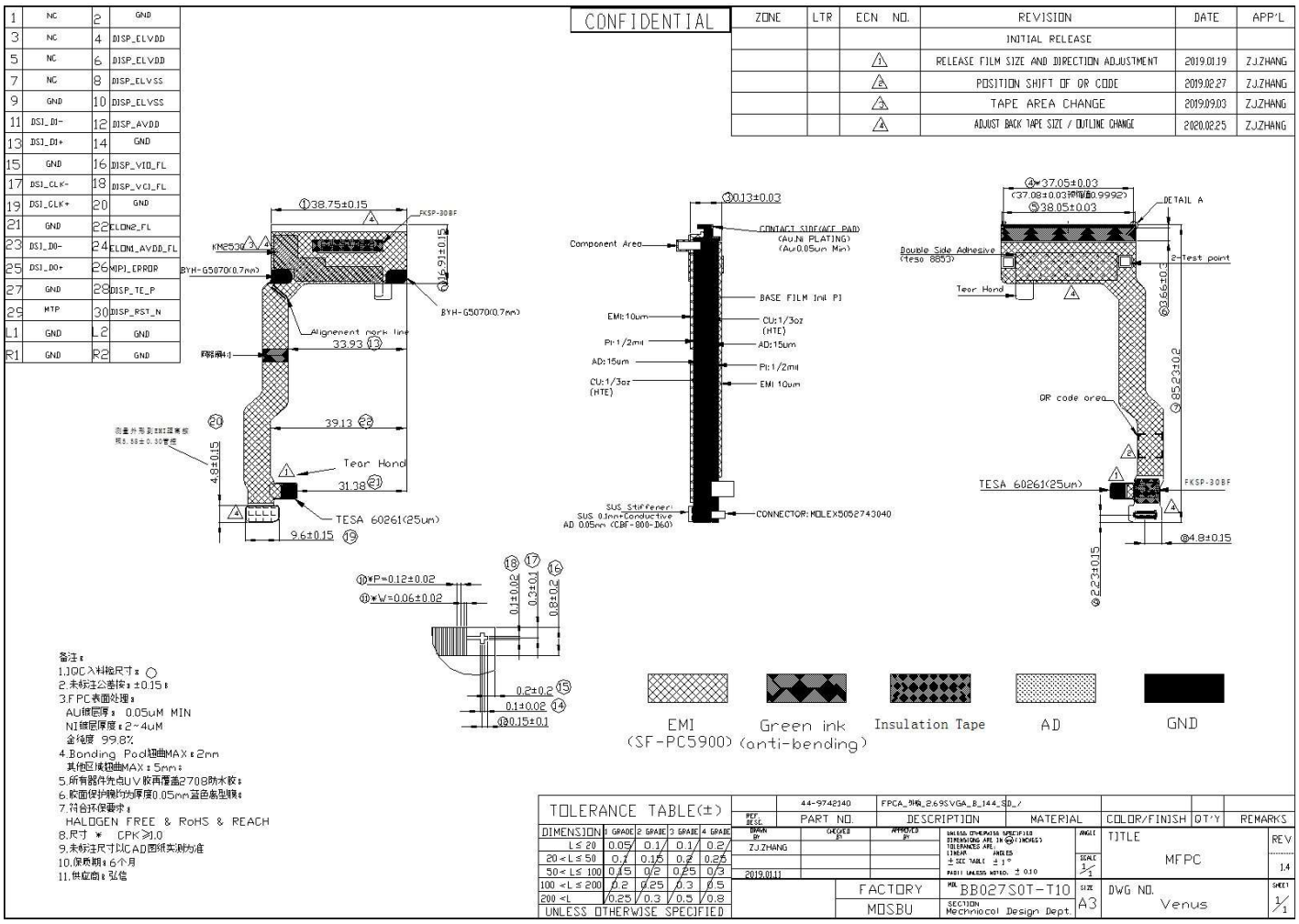


Figure 9.2.3 PVT

9.3 Touch Sensor Drawing

9.3.1 TSP FPC Schematic Diagram

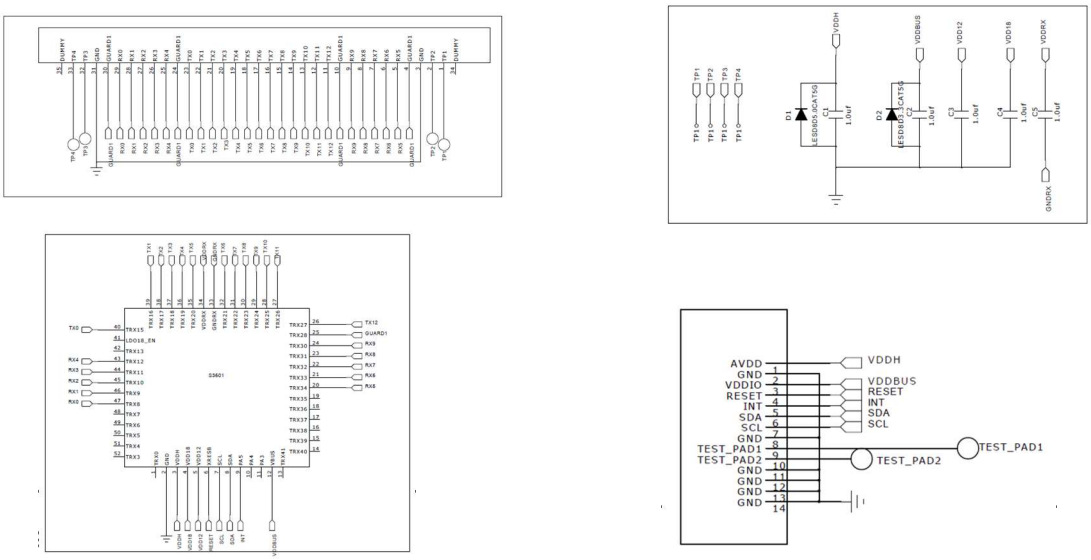


Figure 9.3.1

9.3.2 TSP FPC Electronic Part List

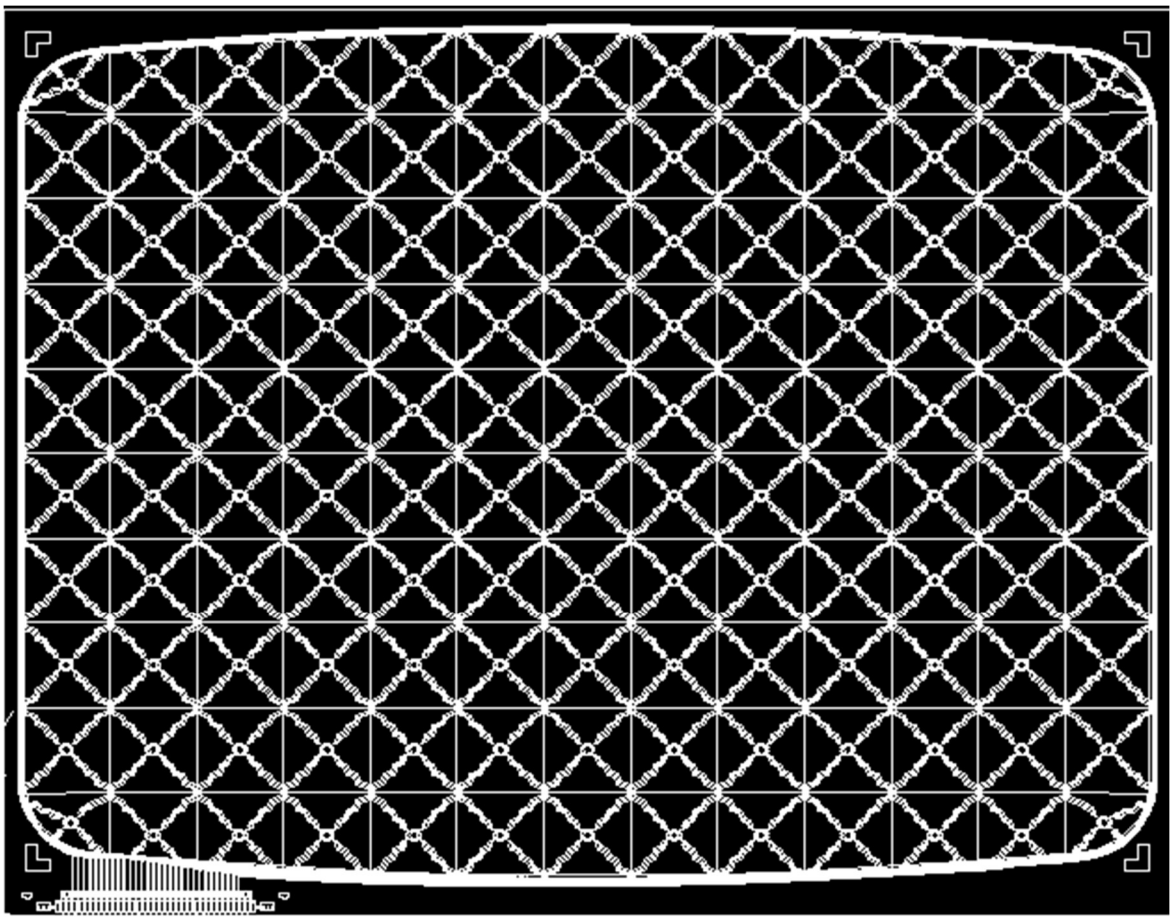


Figure 9.3.2

Table 9.3.2

TFPC					
Comment	Description	Designator	Footprint	Quantity	Value
Cap	Capacitor	C3/C4	0402	2	1uF/6.3V
Cap	Capacitor	C2	0402	1	1uF/6.3V
Cap	Capacitor	C1/C5	0402	2	1uF/10V
Diode	Diode	D1/NC	LESD8D5.0CAT5G	1	NC
Diode	Diode	D2/NC	LESD8D3.3CAT5G	1	NC
u1	Connector		MOLEX559099872	1	
T-IC	Touch IC		S3601	1	

9.3.3 TSP FPC Placement

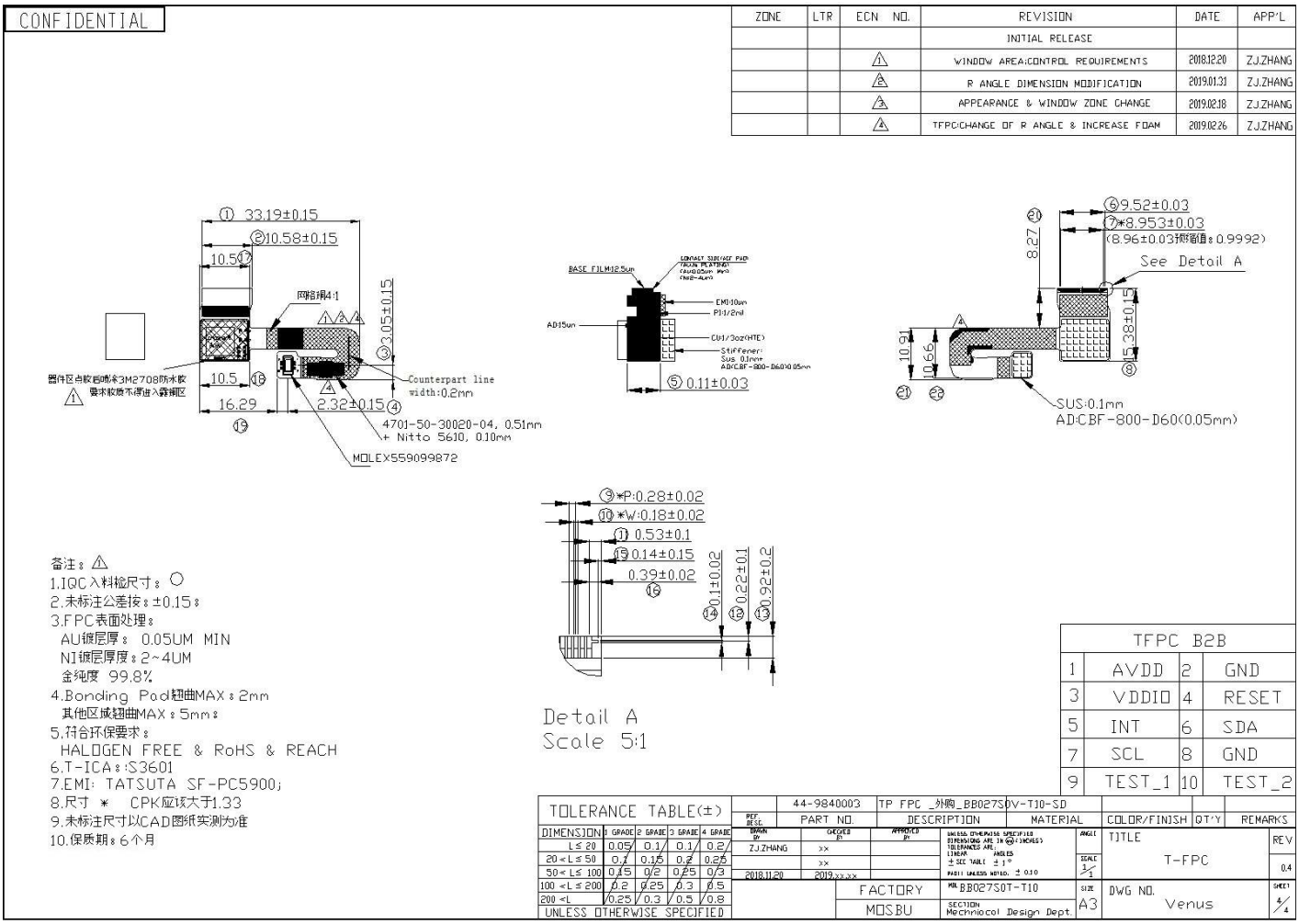


Figure 9.3.3

10. Reliability

10.1 Environmental test

Table 10.1

No.	Item	Condition	Qnty	Result	Judgment Criterion
1	HTS	80℃,240hr	5 ea	OK	1. In the process of the test sample to work properly, no dysfunction。 2. The test is finished, return to room temperature, the sample appearance, display function is normal, no new display abnormal。
2	LTS	-40℃,240hr	5 ea	OK	
3	THS	60℃/90%RH,240hr	5 ea	OK	
4	HTO	70℃,240hr	5 ea	OK	
5	LTO	-20℃,240hr	5 ea	OK	
6	TST	-40℃~80℃, 60 Cycles	5 ea	OK	

10.2 Other test

Table 10.2

No.	Item		Condition	Qnty	Result	Judgment Criterion
1	ESD	Front on display	±4KV(Contact)/ ±8kV(Air), 150pF/330Ω	5 ea	OK	In the process of the test sample to work properly, no dysfunction。

11. Handling Precautions

11.1 Mounting Method

The AMOLED panel module consists of two slim glasses with polarizer which can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board. Extreme care should be used when handling the AMOLED modules.

11.2 Caution of AMOLED Handling and Cleaning

When cleaning the display surface, use soft cloth solvent as recommended below and wipe gently.

- Isopropyl alcohol
- Ethyl alcohol
- Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent.

- Water
- Ketone
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns. Do not use the following solvent on the pad and prevent it from being contaminated.

- HCFC (Other area except ITO pad can use the HCFC for cleaning process)
- Soldering flux
- Chlorine(Cl), Sulfur(S)
- Spittle, Fingerprint

If the product is not wrapped with a desiccant added pad, ITO pattern can be damaged by corrosion. Good Display suggests wrapping a product with a desiccant unless customers particularly indicate that they do not want it. In case ITO pattern corrodes due to the usage of chlorine, sulfur or customer's mishandling of the product, the responsibility lies with the customer.

11.3 Caution against Static Charge

For AMOLED module, use C-MOS LSI drivers, therefore we recommend that you ; Connect any unused input terminal to VCI or VSS, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects AMOLED. Against static charge, you should make sure that the product is safe or not by experiment in advance.

11.4 Packing

- The packing principle is that AMOLED module should keep its packing condition at the time of delivery.
- For safety & avoiding the module damage, Carton box must stack the below 4 boxes. When storing the AMOLED after unpacking, note the followings.
- AMOLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.
- To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

11.5 Caution for Operation

- If you do not follow normal POWER ON, OFF sequence or abnormal operating, then AMOLED module can be damaged electro-optically and does not recover. Do not change software without Good Display confirmation.
- Response time may extremely delay at a temperature lower than operating range; AMOLED does not normally operate at a high temperature. But this may recover at a proper temperature.
- When you set optimal operating voltage to AMOLED module, you can see the optimal contrast of AMOLED. So, add voltage controllable function at SET Module.
- AMOLED module may not display normally when twisting power or pressing power is added. Therefore you should secure AMOLED module maximum thickness at set assembly not to have any pressure affect AMOLED module.
- Electro-chemical reaction may occur when there is humidity on pad; therefore, you should use AMOLED Module below maximum operating humidity.

- AMOLED Module Power Vdd should be designed to protect surge current at SET Module.
- You should not damage connector and cable for AMOLED module assembly by force folding or by applying extreme power.
- AMOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage AMOLED module by surrounding elements.
- To satisfy EMI standards, you should plan your design after considering emitting energy.
- We cannot guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area.
- Image-sticking may occur if AMOLED displays same image for a long time, so you need to make a change for AMOLED.
- When remove the window protective film, necessarily need to apply as a way to prevent Cushion and conductive tape Delamination.

  - As an upper Figure, the handler takes off the direction of the arrow to remove the protective film.

11.6 Storage

- Place in a dark place where neither exposure to direct sunlight nor any fluorescent light is permitted and keep at room temperature & room humidity.
- Store with no contact with polarizer surface.

  [It is recommended to store them as they have been contained in the inner container when we delivered them.

11.7 Safety Precautions

- Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part.
- In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary.
- Do not use the AMOLED module for the special purpose besides display units.
- Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken.
- For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

12. Packing Specification

12.1 Box Pack

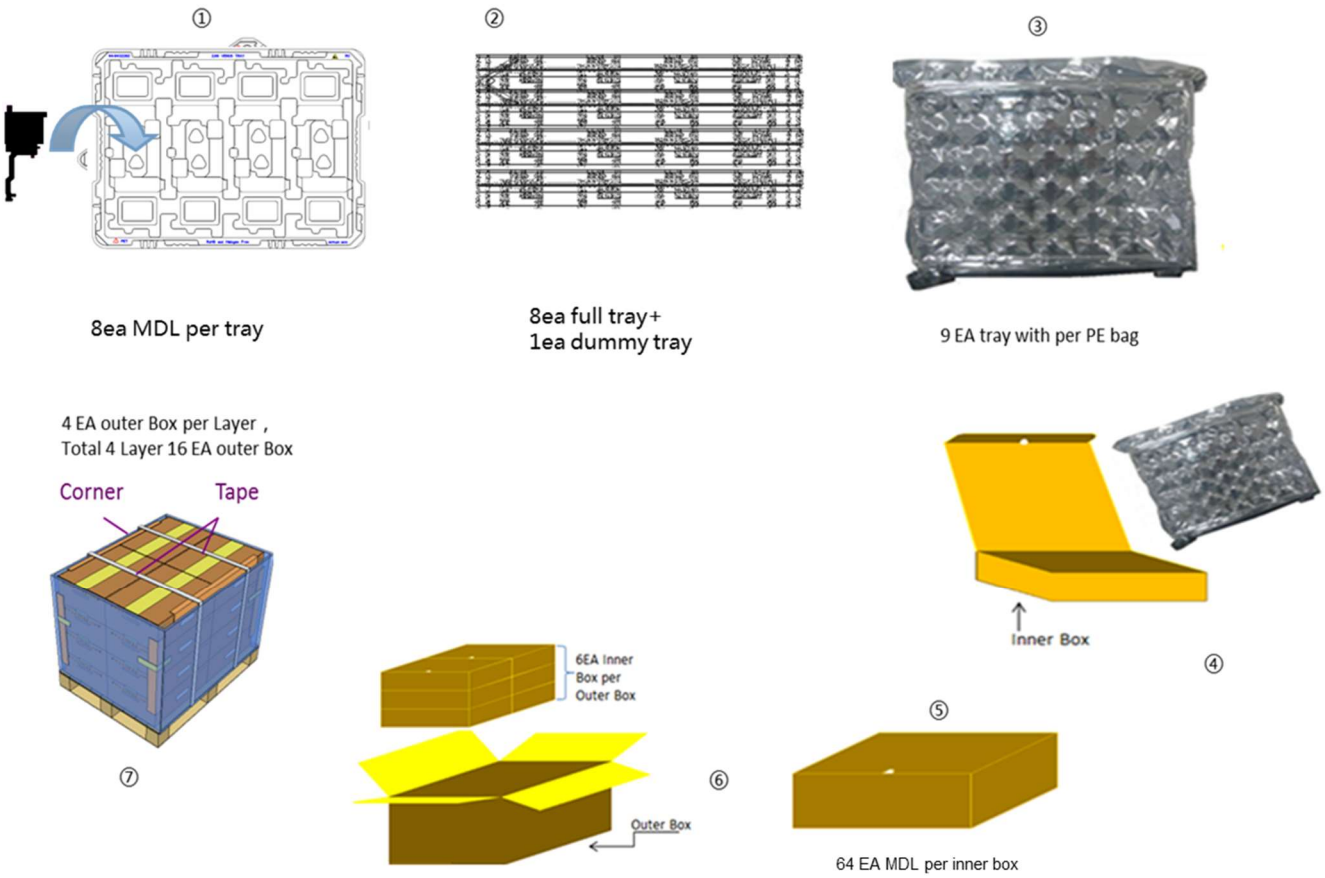


Figure 12.1