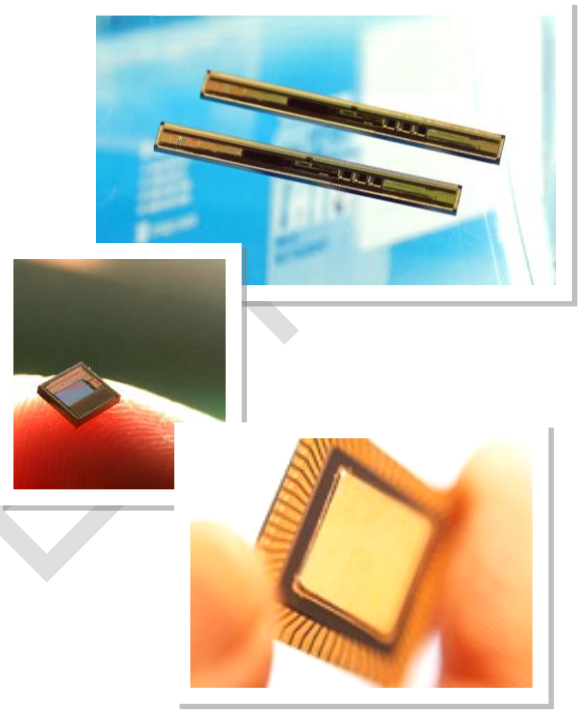
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM69700 Datasheet

Single Chip Driver with 16.7M color

for 1600RGBx2560 OLED driver

Revision：0.4

Date：Mar. 19, 2018

Revision History

Version	Date	Description	Page
0.1	2017/8/29	First release	
0.2	2017/10/27	1. To add voltage step description for VGMP/VGSP/VREFP/VREFN/ OVDD_INT/OVSS_INT 2. To add note for IM[0] pin 3. To add PPS section 4. To add MIPI data type table 5. To add restriction for 2C00h and 3C00h 6. To correct typo in Absolute Maximum Ratings 7. To add Timing skew between Port A and B 8. To modify timing specification of Video Mode 9. To update power on/off timing parameters and diagram	P8 P13 P35,36 P43,44 P63,71 P101 P109 P112 P115,116
0.3	2017/1/15	To update GOA Pin Assignment bit number To add MTP_PWR Description To update MIPI A/B skew	
0.3	2017/1/23	To add FA00h setting To update FE00h	
0.4	2018/3/19	To add MIPI Video mode format To add MIPI Video mode timing	

Table of Contents

1. General Description

The RM69700 device is a single chip solution for LTPS AMOLED that incorporates gate drivers and is capable of 1600RGBx2560, 1440RGBx2560, 1440RGBx2880, and 1440RGBx3200 operations with embedded GRAM. It utilizes SPR (sub pixel rendering) algorithm to reduce sub-pixel numbers while keeping the same picture quality. In addition to 1600RGBx2560 and 1440RGBx2560 with SPR to emulate WQXGA and WQHD resolution, this LSI also supports real FHD with 1080RGBx1920 resolution. It includes internal frame memory, a timing controller with glass interface level-shifters and a glass power supply circuits.

The RM69700 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments according to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 1400RGBx3200-dot 16.77M-color images.

For the normal operation mode, the built-in auto-current limit and dynamic OLED power control are provided for the power saving. For the standby mode, the deep standby mode is supported for ultra low power consumption.

This LSI is very suitable for small and medium-sized portable mobile solutions requiring long-term driving capabilities especially for cellular phone application.

2. Features

- Single chip with RAM for WQHD/WQHD+/WQXGA AMOLED controller/driver
- Display resolution option
  - WQXGA SPR (1600 x 2 x 2560)
  - WQHD/WQHD+ SPR (1440 x 2 x 2560/ 2880/ 3040/ 3200)
  - FHD Real (1080 x 3 x 1920)
- Channel Option
  - Support 3240/3200/3072/2880/2700/2560/2400/2160ch
- Display mode (Color mode)
  - Full color mode: 16.7M colors (24-bit)
  - Reduce color mode: 262K colors (18-bit)
  - Reduce color mode: 65K colors (16-bit)
  - Idle mode: 8 colors
- Interface
  - 3-wire SPI
  - I2C interface (SCL/SDA)
  - MIPI D-PHY Interface:
    - MIPI 2 ports, total 8 data lanes (Maximum data rate is 1Gbps/lane for HSDT)
    - 2 ports for input data without compression (WQXGA or WQHD)
    - 1 port for input data with 1/3 VESA compression (WQXGA or WQHD)
    - 1 port for input data without compression (FHD only)
- Abundant color display and drawing functions
  - Programmable gamma correction function for 16.7 million color display
  - Individual gamma correction setting for RGB dots
  - Support High Brightness Mode (HBM) function
  - Support Brightness Control
- Color Enhancement
  - Saturation Enhancement
  - Brightness Enhancement
  - Skin-Tone and Local Hue Adjustment
  - 2-Dimensional Sharpness Enhancement
  - Contrast Enhancement
  - White Balance Adjustment
  - High Dynamic Range (HDR)
- Rendering IP
  - Support RGBG and RGB delta types
- Power Saving Mode
  - Auto Current Limitation (ACL)
  - Dynamic ELVSS Control
- Peripheral Control Timing and Power Generator
  - Internal oscillator

- 3240ch source outputs
- Support programmable GOA control
- VGHR/VGLR voltage for GOA control signal
- VREFP/VREFN voltage generator for OLED panel voltage
- Internal Charge Pump for AVEE/VCL/VGH/VGL
- Support S-wire interface for power IC control

■ Miscellaneous Function
- Built-in OTP for adjusting gamma, GOA timing, power setting and etc.
- Support PCD (Panel Crack Detection) function
- Support AOD function with built-in OVDD/OVSS supply
- Support Scaling Up function

■ Operating Condition
- Power Supply Input of Regulator and Interface Logic, VDDI: 1.62V ~ 1.98V
- Power Supply Input for DVDD/MVDDA Regulator, VCC/VDDAM: 1.62V ~ 1.98V
- Power Supply Input for Analog Circuitry, VDDA/VDDB/VDDR=VCI and AVDD:
  VCI=2.7V ~ 3.6V, AVDD: 4.5V ~ 8.0V
- Operating temperature: -40°C ~ 85°C
- Storage temperature: -55°C ~ 125°C

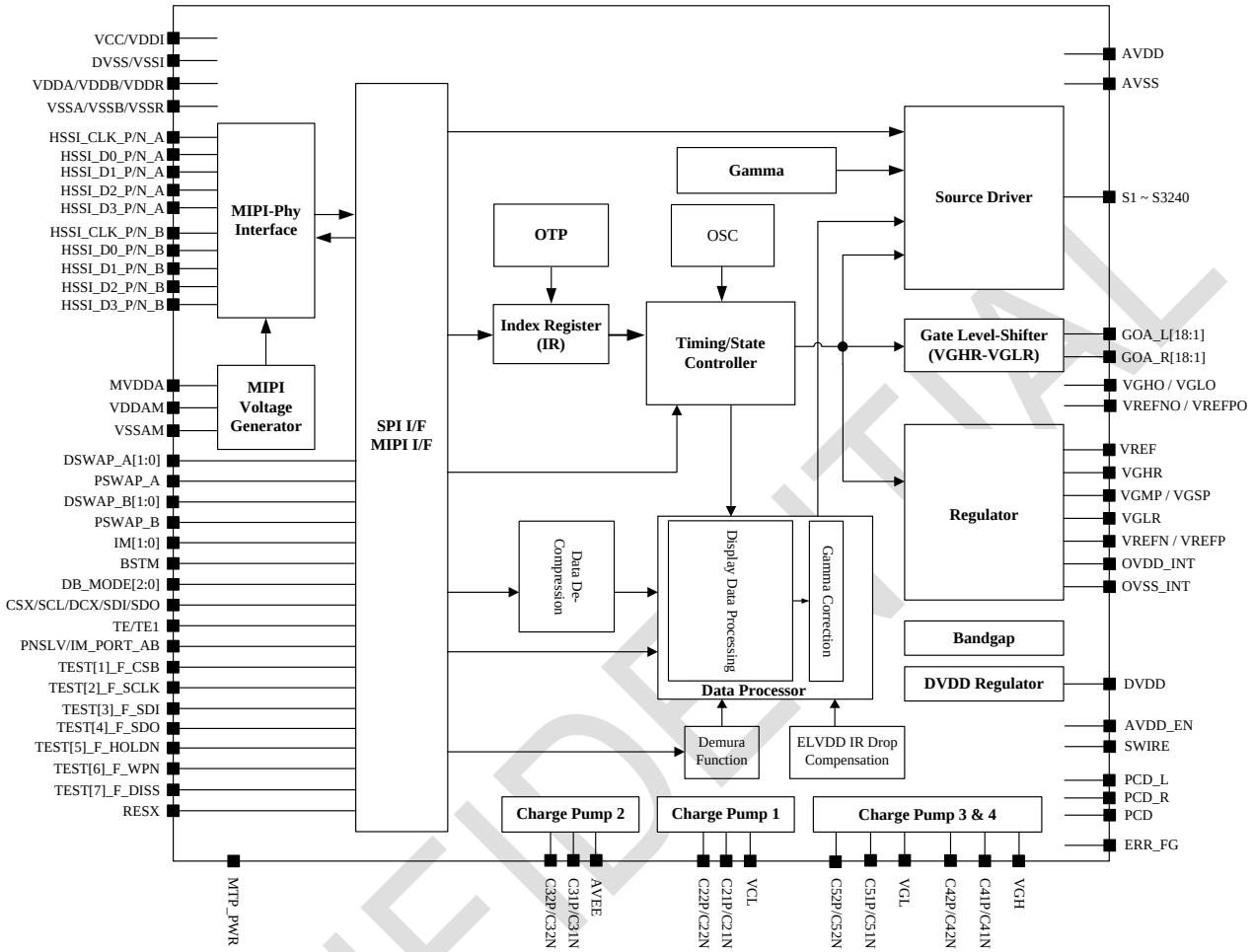
■ Output voltage levels
- Positive gate driver voltage range for VGHR: 3V ~ 15V (Step = 0.1V)
- Negative gate driver voltage range for VGLR: -3V ~ -15V (Step = -0.1V)
- VREFP panel voltage range : 0.2V ~ AVDD-0.3V
  (Step = 0.05V when VREFP<3V and 0.1V when VREFP>3V)
- VREFN panel voltage range : -0.2V ~ AVEE+0.3V
  (Step = -0.05V when VREFN> -3V and -0.1V when VREFN< -3V)
- Gamma high/low voltage range:
  -- VGMP: 2.0V ~ AVDD-0.3V (Step= 12.5mV)
  -- VGSP: 0V, 0.2125V ~ 5V (Step= 12.5mV)
- OVDD_INT/OVSS_INT voltage range for AOD application:
  -- OVDD_INT: 0V, 2.0V ~ 7.6V (Step= 0.1V)
  -- OVSS_INT: 0V, -0.2V ~ -6.4V (Step= -0.1V)

■ Package: COF/COG/COP

■ Power Supply Specifications

No.	Item		Description
1	Source Driver		3240 pins
2	Gate control timing level shift		VGHR - VGLR
3	Input Voltage	VDDI	1.62V ~ 1.98V (typical 1.8V)
		VCC, VDDAM	1.62V ~ 1.98V (typical 1.8V)
		VCI(=VDDA/VDDB/VDDR)	2-Power mode: 2.7V ~ 3.6V
		AVDD	2-power mode: 4.5V ~ 8.0V
4	OLED Drive Voltages	VGMP	2.0V ~ (AVDD-0.3V)
		VGSP	0V, 0.3V ~ (AVDD-1.5V)
		VGHR	3V ~ 15V
		VGLR	-3V ~ -15V
		VREFP	0.2V ~ (AVDD-0.3V)
		VREFN	-0.2V ~ (AVEE+0.3V))
5	Internal Step-Up Circuits	AVEE	AVDD x-1
		VCL	VDDB x-1
		VGH	x3: AVDD + VDDB x4: AVDDx2 x5: AVDD + VDDB -AVEE x6: AVDDx2 - AVEE
		VGL	x-3: AVEE - VDDB x-4: AVEE - AVDD x-5: AVEE - AVDD - VDDB x-6: AVEEx2 - AVDD

3. Block Diagram



4. Pin Description

4.1 Power Supply Pins

Signal	I/O	Function
VDDA	P	Power supply for analog circuitry VDDB, VDDA and VDDR should be the same input voltage level
VDDB	P	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDR	P	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDDI	P	Power supply for interface system except MIPI interface
VDDAM	P	Power supply for interface system of MIPI interface
VCC	P	Power supply for DVDD regulator
VSSA	P	System ground for analog circuitry
VSSB	P	System ground for DC/DC converters
VSSR	P	System ground for regulators
VSSAM	P	System ground for internal MIPI analog circuits
VSSI	P	System ground for interface system except MIPI interface
DVSS	P	System ground for internal digital circuits
AVSS	P	System ground for driver output circuits
MTP_PWR	P	MTP programming power supply pin (6.0V typical) Must be left open or connected to ground in normal condition.
AVDD	P	Power supply for analog circuitry and driver outputs - 2-Power mode, this power is from power IC controlled by AVDD_EN

4.2 SPI/I2C Interface Pins

Signal	I/O	Function
CSX	I	(SPI) Chip select pin to enable SPI interface. If not used, please connect to VSSI.
WRX_SCL	I	(SPI) Synchronous clock input for input data latch. If not used, please connect to VSSI. (I2C) SCL clock input pin
DCX	I	(SPI) Indicator of input data types for 4-wire SPI I/F. If not used, please connect to VSSI.
SDI_RDX	I/O	(SPI) Serial data input signal. If not used, please leave this pin open. (I2C) SDA data pin (selectable input of open-drain)
SDO	O	Serial data output signal. The data is output on the rising/falling edge of the SCL signal. If not used, please leave this pin open.

4.3 MIPI Interface Pins

Signal	I/O	Function
HSSI_CLK_P_A HSSI_CLK_N_A	I	These pins are DSI-CLK+/- differential clock signals of Port -A. If not used, please connect these pins to VSSAM.
HSSI _D0_P_A HSSI _D0_N_A	I/O	These pins are DSI-D0+/- differential data signals of Port-A. If not used, please connect these pins to VSSAM.
HSSI_D1_P_A HSSI_D1_N_A	I/O	These pins are DSI-D1+/- differential data signals of Port-A. If not used, please connect these pins to VSSAM.
HSSI_D2_P_A	I/O	These pins are DSI-D2+/- differential data signals of Port-A. If not used, please connect

<table>
<tr><td>HSSI_D2_N_A</td><td></td><td>these pins to VSSAM.</td></tr>
<tr><td>HSSI_D3_P_A
HSSI_D3_N_A</td><td>I/O</td><td>These pins are DSI-D3+/- differential data signals of Port-A if MIPI interface is used. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_CLK_P_B
HSSI_CLK_N_B</td><td>I</td><td>These pins are DSI-CLK+/- differential clock signals of Port-B. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D0_P_B
HSSI_D0_N_B</td><td>I/O</td><td>-These pins are DSI-D0+/- differential data signals of Port-B. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D1_P_B
HSSI_D1_N_B</td><td>I/O</td><td>-These pins are DSI-D1+/- differential data signals of Port-B. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D2_P_B
HSSI_D2_N_B</td><td>I/O</td><td>-These pins are DSI-D2+/- differential data signals of Port-B. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D3_P_B
HSSI_D3_N_B</td><td>I/O</td><td>-These pins are DSI-D3+/- differential data signals of Port-B. If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>DSWAP_A[1:0]
PSWAP_A
DSWAP_B[1:0]
PSWAP_B</td><td>I</td><td>Input pins to select lane sequence and polarity for D-PHY data transmission:
<table>
<tr><th>PSWAP_A</th><th>DSWAP_A[1:0]</th><th>HSSI_D0_N_A</th><th>HSSI_D0_P_A</th><th>HSSI_D1_N_A</th><th>HSSI_D1_P_A</th><th>HSSI_CLK_N_A</th><th>HSSI_CLK_P_A</th><th>HSSI_D2_N_A</th><th>HSSI_D2_P_A</th><th>HSSI_D3_N_A</th><th>HSSI_D3_P_A</th></tr>
<tr><td>0</td><td>00</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>0</td><td>01</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>0</td><td>10</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>0</td><td>11</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
<tr><td>1</td><td>00</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>1</td><td>01</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>1</td><td>10</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>1</td><td>11</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
<tr><th>PSWAP_B</th><th>DSWAP_B[1:0]</th><th>HSSI_D0_N_B</th><th>HSSI_D0_P_B</th><th>HSSI_D1_N_B</th><th>HSSI_D1_P_B</th><th>HSSI_CLK_N_B</th><th>HSSI_CLK_P_B</th><th>HSSI_D2_N_B</th><th>HSSI_D2_P_B</th><th>HSSI_D3_N_B</th><th>HSSI_D3_P_B</th></tr>
<tr><td>0</td><td>00</td><td>D3-</td><td>D3+</td><td>D2-</td><td>D2+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D0-</td><td>D0+</td></tr>
<tr><td>0</td><td>01</td><td>D0-</td><td>D0+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D2-</td><td>D2+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>0</td><td>10</td><td>D2-</td><td>D2+</td><td>D1-</td><td>D1+</td><td>CLK-</td><td>CLK+</td><td>D0-</td><td>D0+</td><td>D3-</td><td>D3+</td></tr>
<tr><td>0</td><td>11</td><td>D3-</td><td>D3+</td><td>D0-</td><td>D0+</td><td>CLK-</td><td>CLK+</td><td>D1-</td><td>D1+</td><td>D2-</td><td>D2+</td></tr>
<tr><td>1</td><td>00</td><td>D3+</td><td>D3-</td><td>D2+</td><td>D2-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D0+</td><td>D0-</td></tr>
<tr><td>1</td><td>01</td><td>D0+</td><td>D0-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D2+</td><td>D2-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>1</td><td>10</td><td>D2+</td><td>D2-</td><td>D1+</td><td>D1-</td><td>CLK+</td><td>CLK-</td><td>D0+</td><td>D0-</td><td>D3+</td><td>D3-</td></tr>
<tr><td>1</td><td>11</td><td>D3+</td><td>D3-</td><td>D0+</td><td>D0-</td><td>CLK+</td><td>CLK-</td><td>D1+</td><td>D1-</td><td>D2+</td><td>D2-</td></tr>
</table>
Notes:
(1) The voltage levels of these control pins are “1” = VDDI level and “0” = VSSI.
(2) DSWAP[1:0] represent DSWAP_A for port-A and DSWAP_B for port-B, and the settings of these two ports can be different.</td></tr>
<tr><td>PNSLV</td><td>I</td><td>PNSLV is used to determine the port sequence when using MIPI dual port (Default=1’b0).
<table>
<tr><th rowspan="2">PNSLV</th><th colspan="2">Pixel Data from Host</th><th rowspan="2">Command</th></tr>
<tr><th>Port A</th><th>Port B</th></tr>
<tr><td>0</td><td>HSSI_D0_A ~ HSSI_D3_A</td><td>HSSI_D0_B ~ HSSI_D3_B</td><td>HSSI_D0_A ~ HSSI_D3_A</td></tr>
<tr><td>1</td><td>HSSI_D0_B ~ HSSI_D3_B</td><td>HSSI_D0_A ~HSSI_D3_A</td><td>HSSI_D0_B ~ HSSI_D3_B</td></tr>
</table></td></tr>
<tr><td>IM_PORT_AB</td><td>I</td><td>Input pin to select MIPI input port number.
<table>
<tr><th>IM_PORT_AB</th><th>Display Data</th><th>Command</th></tr>
<tr><td>0</td><td>MIPI DSI (Single Port)
HSSI_D0_A ~ HSSI_D3_A</td><td>According to PNSLV</td></tr>
<tr><td>1</td><td>MIPI DSI (Dual Port)
HSSI_D0_A ~ HSSI_D3_A
HSSI_D0_B ~ HSSI_D3_B</td><td>According to PNSLV</td></tr>
</table></td></tr>
</table>

4.4 Interface Logic Pins

Signal	I/O	Function
TE	O	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. This pin is pulled to low when not activated and please leave it open.

<table>
<tr><td>TE1</td><td>O</td><td>Tearing effect output pin to trigger touch events, activated by S/W command. This pin is pulled to low when not activated and please leave it open.</td></tr>
<tr><td>RESX</td><td>I</td><td>Hardware reset pin.</td></tr>
<tr><td>IM[1:0]</td><td>I</td><td>Interface type selection.
<table>
<tr><th>IM[1:0]</th><th>Interface Selection</th></tr>
<tr><td>00</td><td>MIPI D-Phy / I2C</td></tr>
<tr><td>01</td><td>MIPI D-Phy / 3-wire SPI</td></tr>
<tr><td>10</td><td>MIPI D-Phy / I2C</td></tr>
</table>
*IM[0] is internal pulled-low</td></tr>
<tr><td>BSTM</td><td>I</td><td>Power mode selection pins. There is 1bit software control for the power-up sequence of 2-power mode.
<table>
<tr><th>BSTM</th><th>Mode</th></tr>
<tr><td>1</td><td>2-power input mode (VDDI, VCI)
VDDA=VDDB=VDDR=VCI, AVDD is from power IC</td></tr>
<tr><td>0</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>SWIRE</td><td>O</td><td>Swire protocol setting pin of power IC, If not used, please open this pin.</td></tr>
<tr><td>AVDD_EN</td><td>O</td><td>Power IC enable control pin, If not used, please open this pin.</td></tr>
<tr><td>ERR_FG</td><td>O</td><td>Output pin used to monitor display driver state and error status of MIPI’s HSDT</td></tr>
<tr><td>PCD_L, PCD_R</td><td>I</td><td>Input pins used for panel crack detection</td></tr>
<tr><td>PCD</td><td>O</td><td>Panel crack detection output pin</td></tr>
<tr><td>TEST1_F_CSB
TEST2_F_SCLK
TEST3_F_SDI
TEST4_F_SDO
TEST5_F_HOLDN
TEST6_F_WPN
TEST7_F_DISS</td><td>IO</td><td>I/O pins to Flash for Demura function</td></tr>
</table>

4.5 Regulator Outputs and DC/DC Convert Pins

Signal	I/O	Function
C21P, C21N C22P, C22N	I/O	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
VCL	O	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
C31P, C31N C32P, C32N	I/O	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement.
AVEE	O	Output voltage from step-up circuit 2, generated from AVDD. Connect a capacitor for stabilization.
C41P, C41N C42P, C42N	I/O	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
VGH	O	Output voltage from step-up circuit 4. Please connect a capacitor for stabilization.
C51P, C51N C52P, C52N	IO	Capacitor connection pins for the step-up circuit which generate VGL. Connect capacitor as requirement.
VGL	O	Output voltage from step-up circuit 5. Please connect a capacitor for stabilization.

DVDD	O	Regulator output used as power of internal logic circuitry. Please connect a capacitor for stabilization.
MVDDA1 & MVDDA2	O	Regulator output used as power of MIPI's analog circuitry. Please connect a capacitor for stabilization.
VGHR	O	LDO output voltage generated from VGH. Please connect a capacitor for stabilization. When not in use, please open this pin.
VGLR	O	LDO output voltage generated from VGL. Please connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	O	LDO output voltage generated from AVDD for positive gamma high voltage.
VGSP	O	LDO output voltage generated from AVDD for positive gamma low voltage.
VREF	O	Regulator output for internal reference voltage. Please connect capacitor for stabilization.
VREFP	O	Regulator output for VREFP. Please connect capacitor for stabilization.
VREFN	O	Regulator output for VREFN. Please connect capacitor for stabilization.
OVDD_INT	O	Regulator output for OVDD_INT. Please connect capacitor for stabilization.
OVSS_INT	O	Regulator output for OVSS_INT. Please connect capacitor for stabilization.

4.6 Driver Output and Bonding Test Pins

Signal	I/O	Function
S[1] ~ S[3240]	O	Pixel electrode driving output.
SDM[1] ~ SDM[4]	O	Source dummy outputs
GOA_R[18:1] GOA_L[18:1]	O	Control signals of GOA
GOA_DMYL1/2 GOA_DMYR1/2	O	GOA dummy outputs, all of them must be open and connect any two of them is forbidden
VGHO	O	Connected to VGHR internally for panel application. If possible, please connect this pin to VGHR on FPC.
VGLO	O	Connected to VGLR internally for panel application. If possible, please connect this pin to VGLR on FPC.
VREFPO	O	Connected to VREFP internally for panel application. If possible, please connect this pin to VREFP on FPC.
VREFNO	O	Connected to VREFN internally for panel application. If possible, please connect this pin to VREFN on FPC.
DUMMY_R1/R2	I	Dummy pins that are used for COG bonding check. They are internally short.
DUMMY_R3/R4	I	Dummy pins that are used for COG bonding check. They are internally short.
PADA	I	Dummy pins that are used for COG bonding check. They are internally short.
PADB	I	Dummy pins that are used for COG bonding check. They are internally short.
DMY_L1~ DMY_L20	I	Dummy test PADs, all of them must be open and the connect ion of any two of them is forbidden
DMY_R1 ~ DMY_R20	I	Dummy test PADs, all of them must be open and the connection of any two of them is forbidden

4.7 Test Pins

Signal	I/O	Function
DB_MODE[2:0]	I	Test mode selection pins. It is not accessible to user and must be left open.

ANA_TEST[4:1]	O	Analog test pins. They are not accessible to user and must be left open
TEST[16:10] TEST[8]	IO	Digital test pins. They are not accessible to user and must be left open
PL	I	Digital test pin. It is not accessible to user and must be left open.
DE	I	Digital test pin. It is not accessible to user and must be left open.
HS	I	Digital test pin. It is not accessible to user and must be left open.
VS	I	Digital test pin. It is not accessible to user and must be left open.
D[7:0]	I	Dummy PAD, please leave them open
DMY	I	Dummy PAD, please leave them open
DMY_L1~ DMY_L20	I	Dummy test PADs. All of them must be open and connect any two of them is forbidden.
DMY_R1~ DMY_R20	I	Dummy test PADs. All of them must be open and connect any two of them is forbidden.

5. Function Description

5.1 DBI Type-C Serial Interface

The RM69700 supports DBI (Display-Bus-Interface) type-C option-1 and option-3 for the communication with the host. For the option-1, it is a 3-wire 9-bit series interface and consists of the chip enable input (CSX), serial clock input (SCL), serial data Input (SDI), and serial data Output (SDO). For the option3, it is a 4-wire serial interface with one more extra pin DCX than option-1 to indicate the input is data or command. The serial clock (SCL) is used only for the interface communication with the MCU, so it can be stopped when no data transmission is being executed.

For a data write cycle, CSX should be low to indicate that the process of serial data transmission is valid. Then, SCL is driven by the host from high to low to start a valid bit data transmission and then pulled back from low to high for display driver to latch data. A low-high-low transition of SCL forms a complete write cycle of one bit data.

A write sequence is initiated when CSX is driven from high to low and ended once CSX is pulled to high. During a write sequence, host processor can write more than one byte command or data to display module via the interface.

For a data read cycle, host processor reads bit-string data from display module via the interface. For a data read cycle, SCL is first driven from high to low to tell the host to fetch data and then pulled back from low to high to complete a read cycle. The display module outputs information during a read cycle to the data line SDO and the host reads the data at the rising edge of SCL from the data line.

A read sequence is initiated when CSX is driven from high to low and ended when CSX is pulled high. During a read sequence, host processor can read more than one byte of information from the display module. The read sequences of single-byte and multi-byte have a difference at the beginning of data output. For the single-bye output, the data are output to the data line SDO soon after the command transmission is finished. As to the multi-byte output, there is a dummy clock cycle inserted between finish of command transmission and the start of data output to the data line SDO.

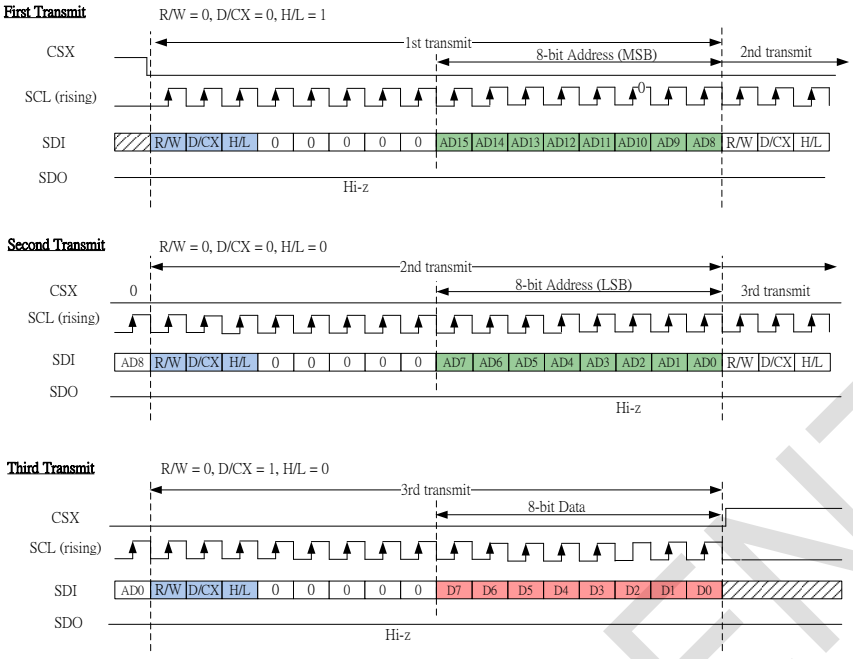
In addition to DBI type-C option-1 and option-3, a 3-wire 16-bit serial interface is also implemented. There are 2-byte data per transmission for this interface. The first 3 MSB bits of the former are R/W, D/CX, and H/L and they are used to tell the driver whether the proceeding transmission is for read (R/W=1) or write (R/W=0), the input is data (D/CX=1) or command (D/CX=0), and the input is the MSB (H/L=1) or LSB (H/L=0).

SPI Interface Type Selection:

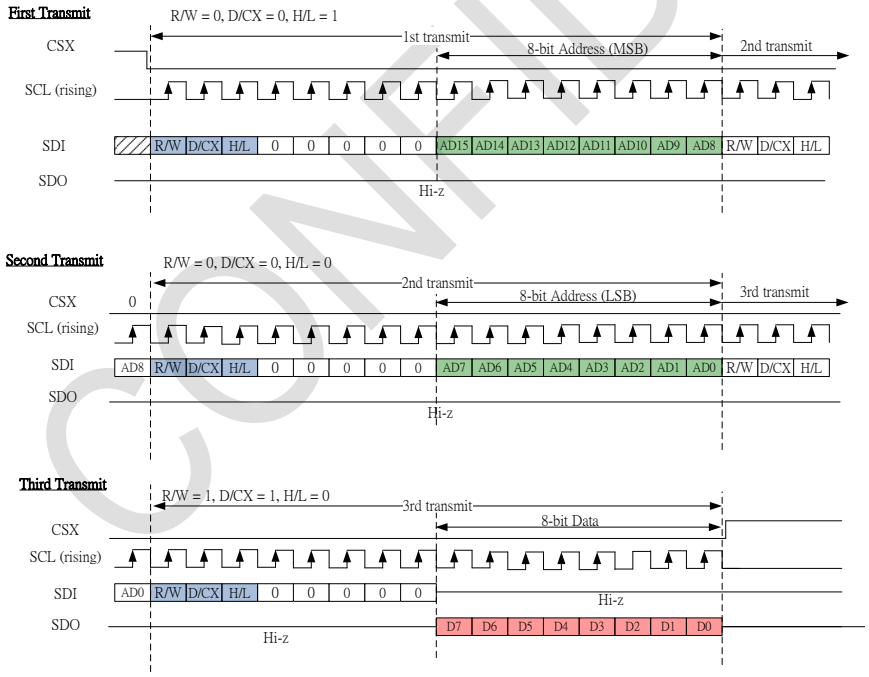
IM[:0]	Display Data	SPI Command
00	MIPI DSI, D-PHY	I2C
01	MIPI DSI, D-PHY	3-wire SPI
10	MIPI DSI, D-PHY	I2C

5.1.1 3-Wire 16-Bit SPI Write/Read Cycle and Sequence

■ **Write sequence**



■ **Read sequence**

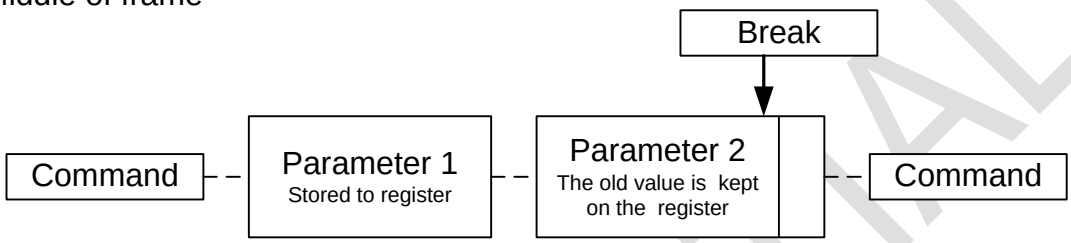


5.1.2 Break and Pause Sequence

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can stop a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before proceeding the read or write sequence at the point where the sequence was paused.

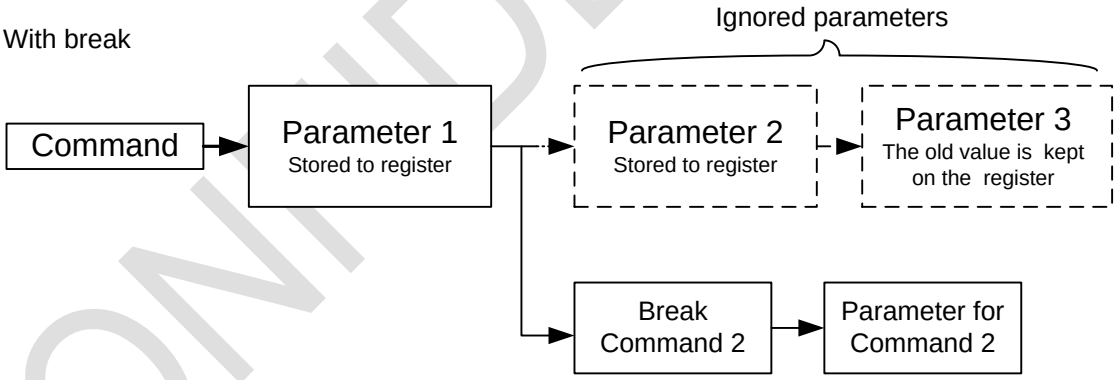
1. Middle of frame



2. Between frames

Without break

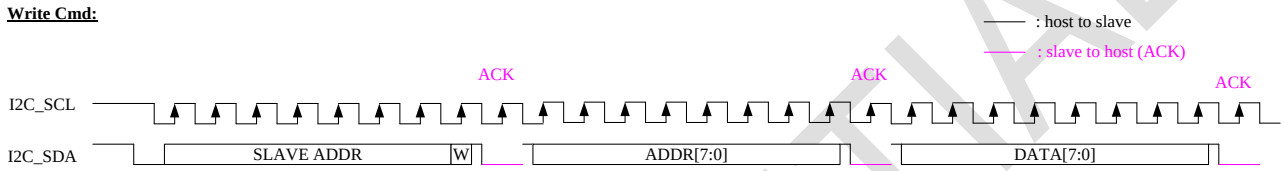
With break



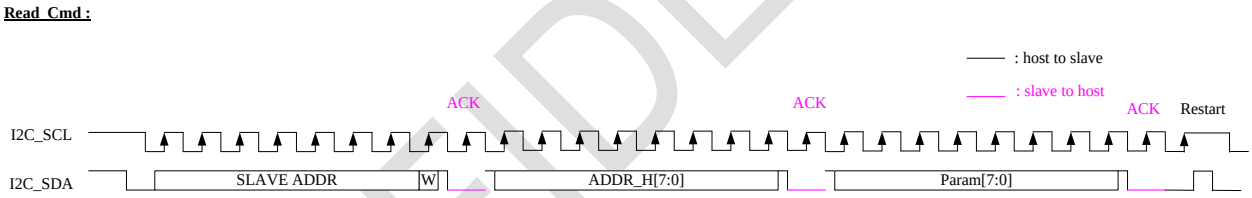
5.2 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I_SDA) and the Serial Clock Line (I_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

The I2C interface write command sequences are described in the following figure.



The I2C interface read command sequences are described in the following figure.



5.3 Display Serial Interface (DSI)

DSI-compliant peripherals support both of two basic modes of operation, *Command Mode* and *Video Mode*. The mode definitions reflect the intended use of DSI for display interconnect but not intend to restrict DSI from operating in other applications.

Command Mode refers to the operation in which transactions primarily take the form of sending commands to a display module, which incorporates a display controller including local registers. It requires a bidirectional interface so that systems can utilize this mode to write data onto or to read data from those local registers. The host processor indirectly controls activity of the peripheral by sending commands and parameters to the display controller. Moreover, the host processor can also read status information of a display module via it.

Video Mode refers to operation in which a real-time pixel stream data send from the host processor to the peripheral. Under normal operation, display module relies on host processor to transmit image data with

sufficient bandwidth to avoid flicker or other visible artifacts shown in the displayed image. Video information should only be transmitted by using High Speed Mode.

Configuration between the host and RM69700 (Slave)

Lane Pair	Available Operation Mode	Clock/Data Input Mode
Clock Lane	Unidirectional Clock Lane	Forward High-Speed Clock Input
Data Lane 0	Bi-directional Data Lane Bi-directional Escape Mode	Forward High-Speed Data Input Bi-directional LPDT
Data Lane 1	Unidirectional Data Lane Escape Mode	Forward High-Speed Data Input No LPDT
Data Lane 2	Unidirectional Data Lane Escape Mode	Forward High-Speed Data Input No LPDT
Data Lane 3	Unidirectional Data Lane Escape Mode	Forward High-Speed Data Input No LPDT

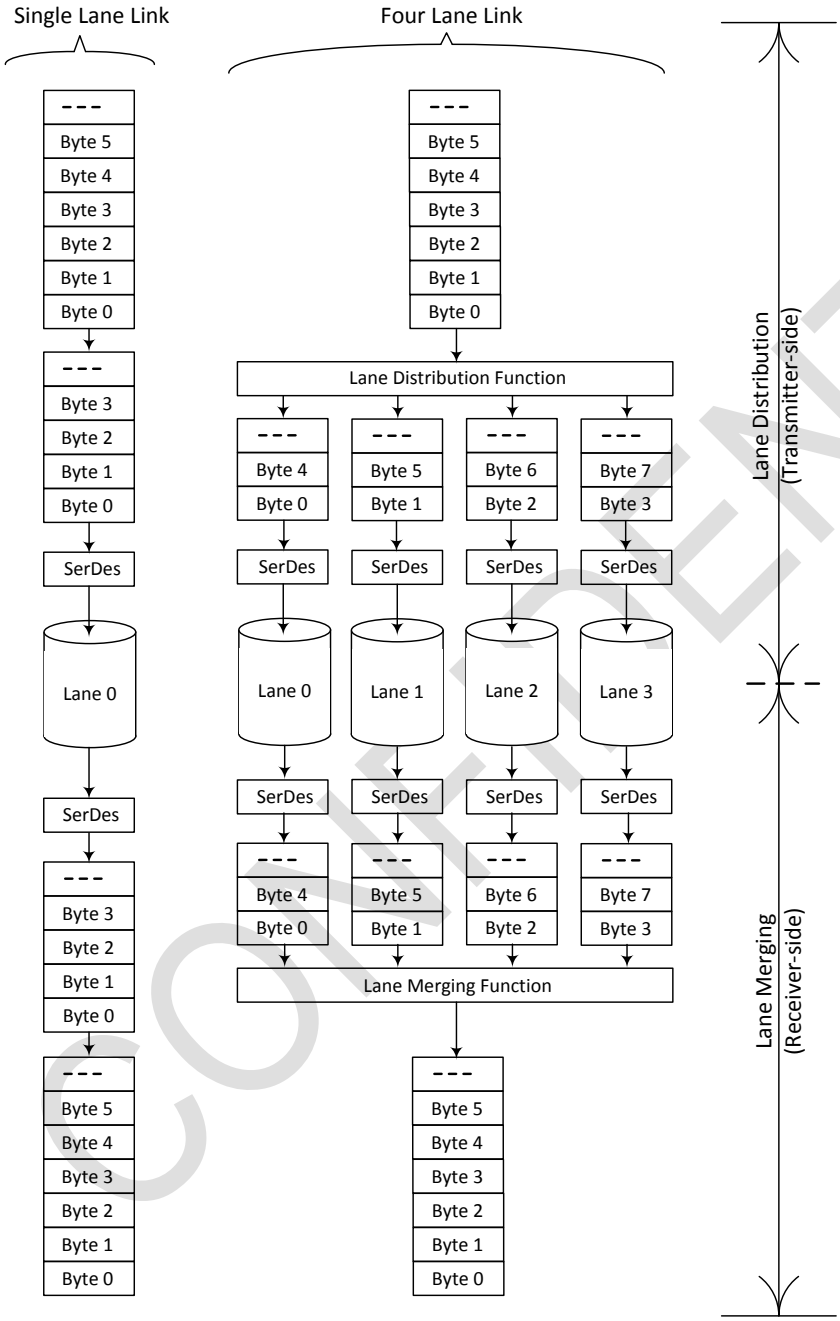
Notes:
1. We recommend users to stay in *STOP* state for 500ns when switching from LPDT to HSDT.
2. We recommend users to adopt *EoTp* to enhance overall robustness of the system during HSDT.

5.3.1 Video Mode Format Support

Video Mode	Support
Burst mode	Yes
Non burst mode	Yes
Sync event mode	Yes
Sync pulses mode	Yes

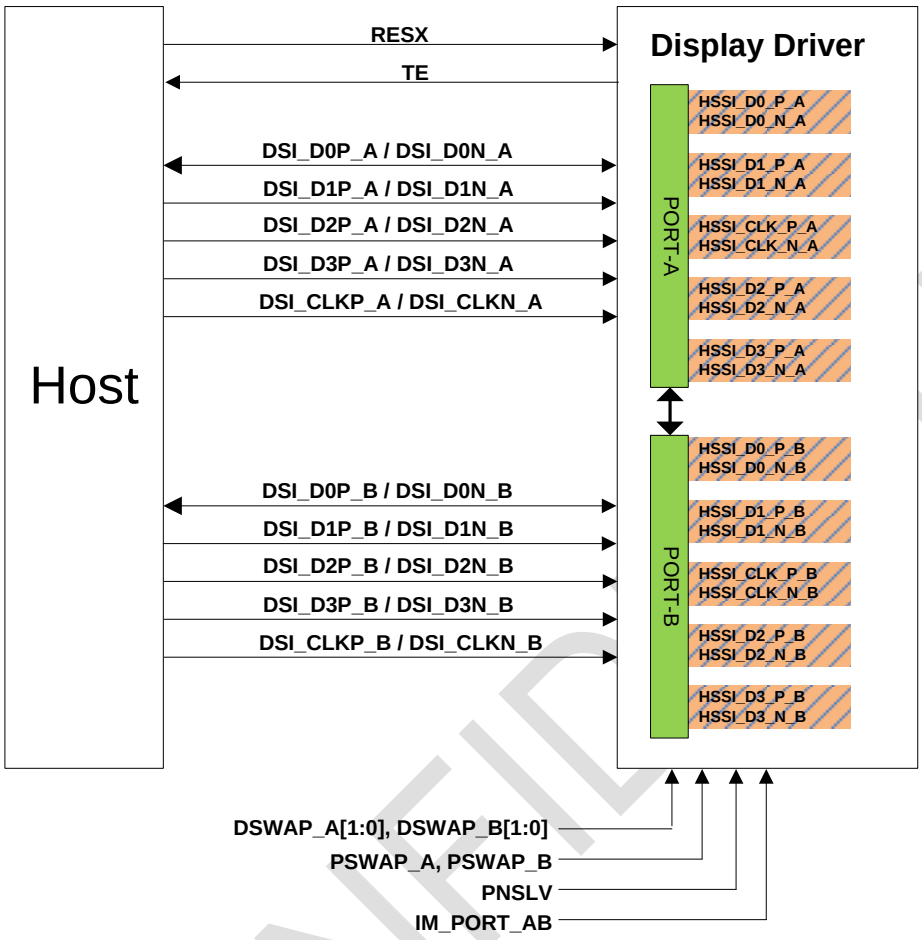
5.3.2 Multi-Lane Distribution and Merging

On the transmitter side of a *DSI Link*, parallel data, signal events, and commands are converted to packets and sent across the serial Link. On the other hand, the receiver side of a *DSI Link* performs the data conversion, decomposing deceived packets into parallel data, signal events and commands. The data processing flow is shown in the following for one-lane operation (left-side) and four-lane operation (right-side).



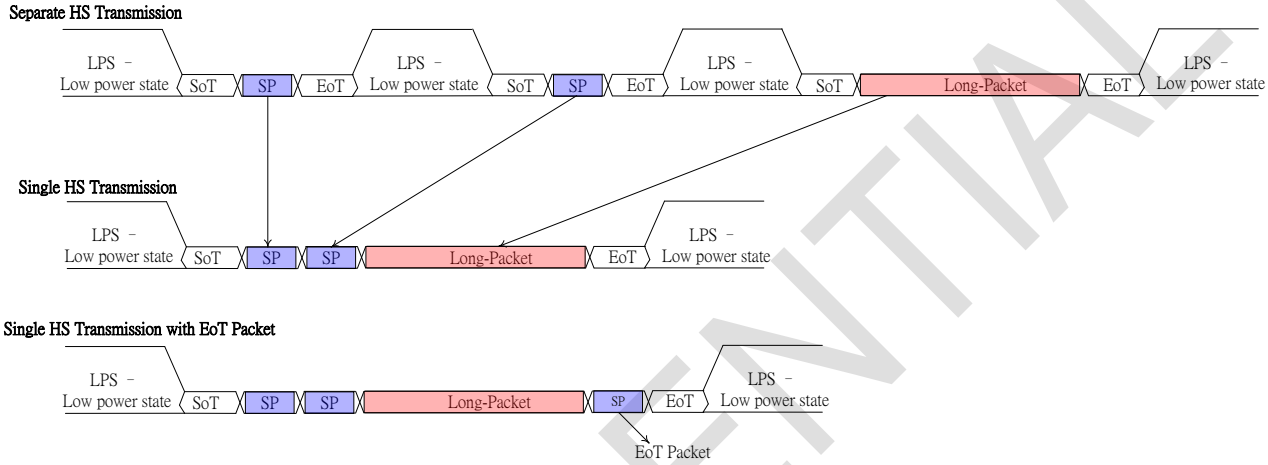
5.3.3 DSI System Configuration

The system configuration is shown as follows. The hardware pin PNSLV select the data port mapping between the host and display driver, and IM_PORT_AB set the valid port number is 1 port or 2 ports. Each port has its own DSWAP and PSWAP for their lane configuration.



5.3.4 Multiple Packet per Transmission

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS data transmission can be started, the transmitter issues a SoT sequence to the receiver. After that, data or command packets can be transmitted via HS mode. Multiple packets may exist within a single HS transmission and at the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In HS mode, time gaps between packets shall result in separate HS transmissions for each packet, with a SoT, LPS, and EoT issued by the PHY layer between packets.



Operation State:

LPS -- Low Power State (also called LP-11)

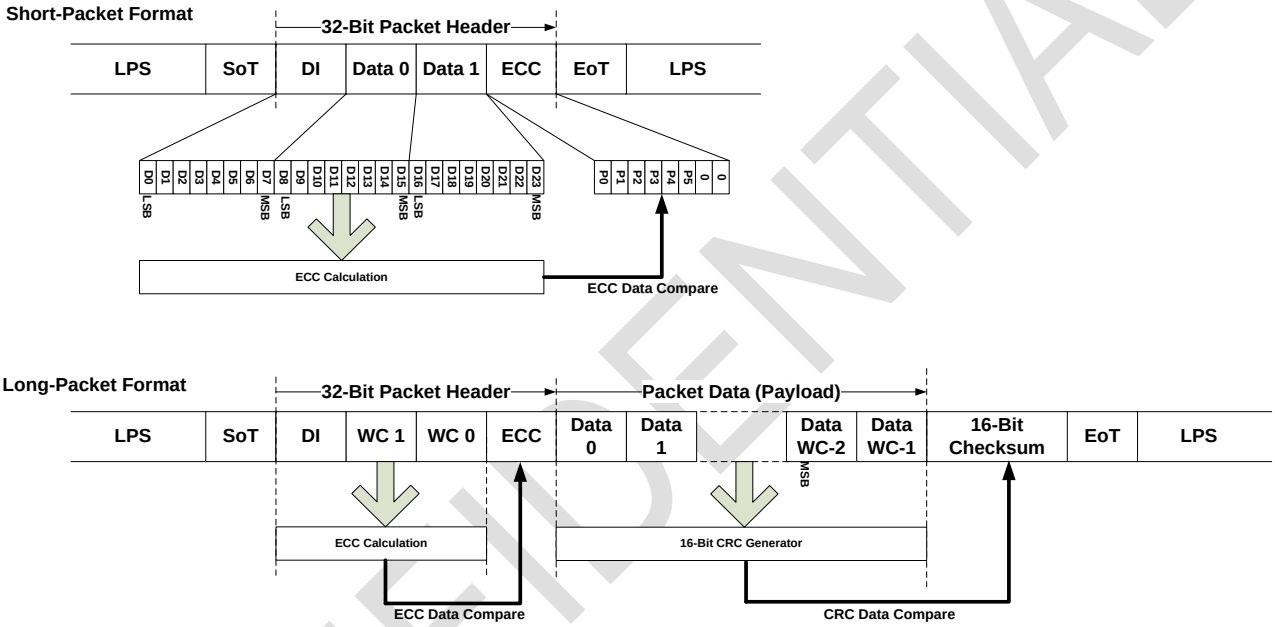
SoT -- Start-of-Transmission

EoT -- End-of-Transmission

5.3.5 Packet Composition

There are two categories of packet size, and they are *short* packets and *long* packets, respectively. Short packets are four bytes in length including the 1 byte DI (data identifier), 2 byte data, and 1 byte ECC (error correction code) for the packet header.

As to the long packets, they comprise of 1 byte DI, 2 byte WC (word count), Data 0, Data 1…Data WC-1, and finally 2 byte checksum. *Word Count* represents the number of total data bytes of this long packet, and *Checksum* is a 16-bit CRC generator to check packet data. If the calculated checksum of receiver is equal to the number contained in the packet, then those packet data are regard as correct. However, if the comparison result is non-equal, the packet data are considered to be incorrect. The packet formats of both short packet and long packet are depicted in the following.



The byte DI[7:0] (data identifier) contains of two important information. One is the peripheral selection through the 2-bit virtual channel identifier VC=DI[7:6], and the other is the 6-bit data type field DT=DI[5:0]. The VC is always 2'b00 for the real application. The data type field specifies the short or long packet type and the packet format.

Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ECC shall always be generated and appended in the Packet Header from the host processor. Peripherals with Bidirectional Links shall also generate and send ECC. The byte ECC allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

The number of parity or error check bits required is given by the Hamming rule, which uses parity to correct a single-bit error or detect a two-bit error, but are not capable of doing both simultaneously. DSI uses Hamming-modified codes where an extra parity bit is used to support both single error correction as well as two-bit error detection.

Since Packet Headers are fixed at four bytes (twenty-four data bits and eight ECC bits), P6 and P7 of the ECC byte are unused and shall be set to zero by the transmitter. The receiver shall ignore P6 and P7 and set both bits to zero before processing ECC. The parity bits of ECC are defined as below:

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

ECC Parity Generation Rules, the encoding of parity and decoding of syndromes:

Data Bit	P7	P6	P5	P4	P3	P2	P1	P0	Hex
0	0	0	0	0	0	1	1	1	0x07
1	0	0	0	0	1	0	1	1	0x0B
2	0	0	0	0	1	1	0	1	0x0D
3	0	0	0	0	1	1	1	0	0x0E
4	0	0	0	1	0	0	1	1	0x13
5	0	0	0	1	0	1	0	1	0x15
6	0	0	0	1	0	1	1	0	0x16
7	0	0	0	1	1	0	0	1	0x19
8	0	0	0	1	1	0	1	0	0x1A
9	0	0	0	1	1	1	0	0	0x1C
10	0	0	1	0	0	0	1	1	0x23
11	0	0	1	0	0	1	0	1	0x25
12	0	0	1	0	0	1	1	0	0x26
13	0	0	1	0	1	0	0	1	0x29
14	0	0	1	0	1	0	1	0	0x2A
15	0	0	1	0	1	1	0	0	0x2C
16	0	0	1	1	0	0	0	1	0x31
17	0	0	1	1	0	0	1	0	0x32
18	0	0	1	1	0	1	0	0	0x34
19	0	0	1	1	1	0	0	0	0x38
20	0	0	0	1	1	1	1	1	0x1F
21	0	0	1	0	1	1	1	1	0x2F
22	0	0	1	1	0	1	1	1	0x37
23	0	0	1	1	1	0	1	1	0x3B

5.3.6 Processor-to-Peripheral Transactions

- **Sync Event packet**

Sync Events are all short packets and time-accurately. They can perform like the start and end of sync pulses. To represent timing information as accurately as possible, a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Hence, a V Sync End event implies an H Sync Start event for the last line of the VSA. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty if keeping data line(s) in HS mode.

Data Type	Data Type (Binary)	Description	Packet size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short

- **End-of-Transmission EoT packet**

This short packet is used to indicate the end of a high speed (HS) transmission, and it will enhance overall system reliability. Although the main objective of the EoT packet is to enhance robustness of HS transmission, DDI can also detect and interpret arriving EoT packet even in LP mode.

Data Type	Data Type (Binary)	Description	Packet size
08h	00 1000	End of Transmission packet (EoTp)	Short

- **Color Mode Off / On Command packet**

They are short packet commands to switch video display module between normal display mode and 8-color mode for power saving.

Data Type	Data Type (Binary)	Description	Packet size
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short

- **Generic Short Write / Read packet**

Generic Short WRITE request is a short packet for sending data to the peripheral. Generic READ request is a short packet for acquiring data from the peripheral.

Data Type	Data Type (Binary)	Description	Packet size
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short

■ **DCS Short Write / Read packet**

DCS short write command is used to write a single data byte command to display module. If there is a valid parameter byte, data type bit 4 shall be set to 1. If there is no valid parameter byte, data type bit 4 shall be set to 0 and the parameter byte shall be 00h. DCS read command is used to request data from DDI.

Data Type	Data Type (Binary)	Description	Packet size
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short

■ **Generic Long Write**

This is used to transmit arbitrary blocks of data from a host processor to a peripheral.

Data Type	Data Type (Binary)	Description	Packet size
29h	10 1001	Generic Long Write	Long

■ **DCS Long Write**

The commands are used to send larger blocks of data to a display module.

Data Type	Data Type (Binary)	Description	Packet size
39h	11 1001	DCS Long Write / write_LUT Command Packet	Long

■ **Set Maximum Return Packet Size**

This command specifies the maximum size of the payload in a long packet transmission from a display module to host processor.

Data Type	Data Type (Binary)	Description	Packet size
37h	11 0111	Set Maximum Return Packet Size	Short

■ **Null Packet**

This is a mechanism for keeping the data lane(s) in high speed mode while sending dummy data.

Data Type	Data Type (Binary)	Description	Packet size
09h	00 1001	Null Packet, no data	Long

■ **Blanking Packet**

A Blanking packet is used to convey blanking timing information in a Long packet. The packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Blanking packets may contain arbitrary data as payload.

Data Type	Data Type (Binary)	Description	Packet size
19h	01 1001	Blanking Packet, no data	Long

■ **Reserved Data Packet**

Data Type	Data Type (Binary)	Description	Packet size
22h	10 0010	reserved	Short
32h	11 0010	reserved	Short
03h	00 0011	reserved	Short
04h	00 0100	reserved	Short

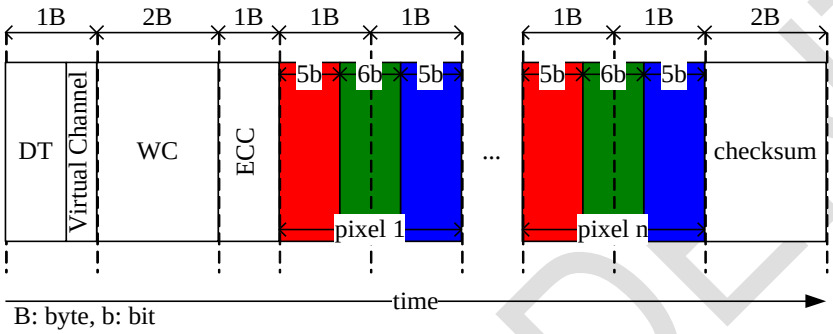
5.3.7 Packed Pixel Stream Format

There are 4 kinds of data input formats, and they are 16-bit RGB(5-6-5),18-bit RGB(6-6-6), loosely packed 18-bit RGB(6-6-6), and 24-bit RGB(8-8-8) data format. They have their own data type as shown in the following table.

Data Type	Data Type (Binary)	Description	Packet size
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

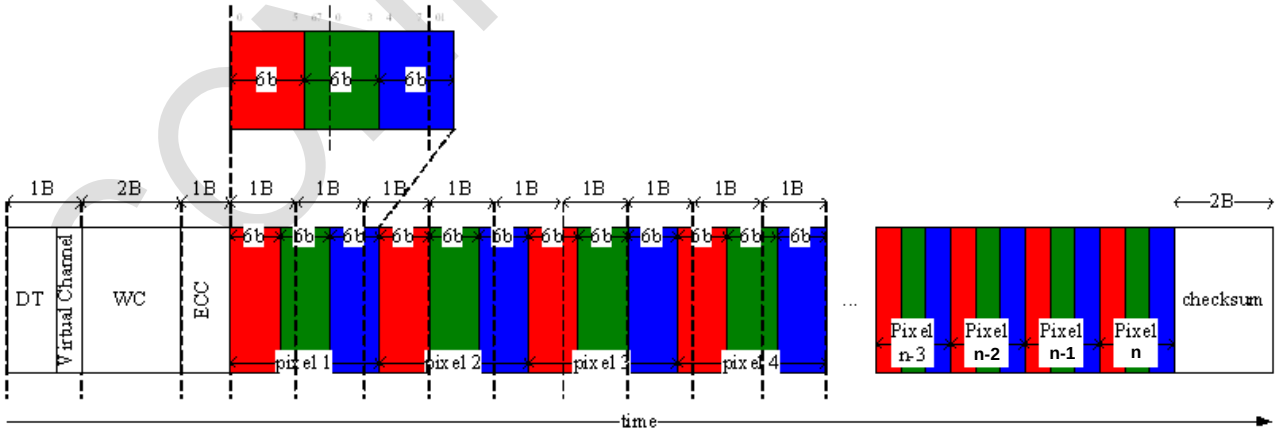
■ **16-bit Format, Data Type: 0x0Eh**

The pixel data of this 16-bit data format comprise of five bits red, six bits green, and five bits blue. The green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.



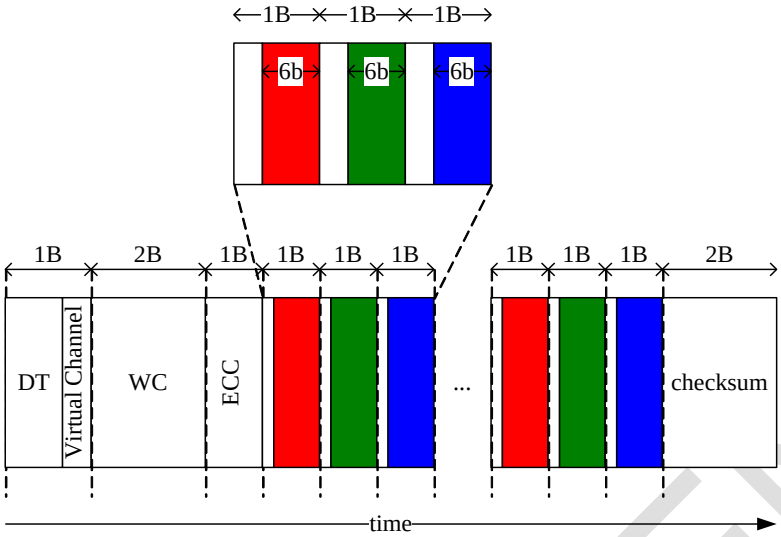
■ **18-bit Format, Data Type: 0x1Eh**

The pixel data of this 18-bit data format comprise of six bits red, six bits green, and six bits blue. Within a color component, the LSB is sent first, the MSB last.



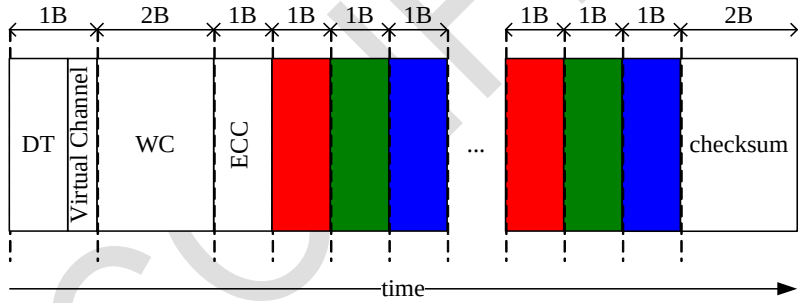
■ 18-bit Loosely Packed Format, Data Type: 0x2Eh

The pixel data of this 18-bit pixel loosely packed format comprises of six bits red, six bits green, and six bits blue. But, the difference between this format and previously mentioned compact format is each R, G or B color component is the same six bits but shifted 2bits to the upper bits of byte. Within a color component, the LSB is sent first, the MSB last.



■ 24-bit Format, Data Type: 0x3Eh

The pixel data of this 24-bit data format is eight bits red, eight bits green and eight bits blue. Within a color component, the LSB is sent first, the MSB last.



5.3.8 Peripheral-to-Processor (Reverse Direction) LP Transactions

All command-mode systems require bidirectional capability to transmit and receive READ data, acknowledge, error information and etc. to the host processor. Multi-Lane system shall use Data Lane-0 for all peripheral-to-processor transmission. And the transmission is allowable only under low-power mode.

Packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction, *Short* and *Long* packet structures. BTA sequence, that is used to pass the bus control from one to the other, shall take place soon after every peripheral-to-processor transaction. There are four major data transmission from a peripheral to its processor:

- *Tearing Effect.* It is a Trigger message sent to convey display timing information to the host processor.
- *Acknowledge*. It is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication, either triggers or packets, is received by the peripheral with no errors. Please refer to section 6.2.5 for the detailed description.
- *Acknowledge and Error Report*: It is a Short packet sent if any errors were detected in preceding transmissions from the host processor. Please refer to section 6.2.6 for the detailed description.
- *Response to Read Request*. It may be a Short or Long packet that returns data requested by the preceding READ command from the processor. Please refer to section 6.2.7 for the detailed description.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packets, and then return bus control to the host processor. Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- Following a non-Read command, the peripheral shall respond with *Acknowledge* if no errors were detected or stored since the last peripheral to host communication.
- Following a Read request, the peripheral shall send the requested READ data if no errors were detected and stored since the last peripheral to host communication.
- Following a Read request, if only a *single-bit ECC error* was detected and corrected, the peripheral shall send the requested READ data in a long or short packet, followed by a 4-byte *Acknowledge and Error Report* packet in the same LP transmission.
- Following a non-Read command, if only a *single-bit ECC error* was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte *Acknowledge and Error Report* packet.
- Following a Read request, if multi-bit ECC errors were detected and not corrected, the peripheral shall send a 4-byte *Acknowledge and Error Report* packet without sending Read data.
- Following a non-Read command, if multi-bit ECC errors were detected and not corrected, the peripheral shall not execute the command, and shall send a 4-byte *Acknowledge and Error Report* packet.
- Following any command, if SoT Error, SoT Sync Error, or DSI VC ID invalid or DSI protocol violation was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte *Acknowledge and*

Error Report response, with the appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication, in the two-byte error field.

- Following any command, if EoT Sync Error or LP Transmit Sync Error is detected, or a checksum error is detected in the payload, the peripheral shall send a 4-byte *Acknowledge and Error Report* packet with appropriate error flags set, as well as any error bits from any preceding transmissions stored since the last peripheral to host communication.

Acknowledge and Error Report confirms that the preceding command or data sent from the processor to a peripheral was received and indicates what type of error detected on the transmissions. Error report is of short packet type that comprised of two bytes following the data identifier byte (Byte-0). An ECC byte (Byte-3) follows the two error report bytes to form a complete short packet. By convention, detection and reporting of each error type is signified by setting the corresponding bit to “1”. The following table shows the bit assignment for all error report:

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

5.3.9 Peripheral-to-Processor Transaction – Detail Format Description

- ***Acknowledge and Error Repor***t

It is sent in response to any command, or read, request, with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

Data type (hex)	Description	Packet size
02h	Acknowledge and Error Report	Short

- ***Generic Short Read Response***

It is a short-packet response to *Generic READ Request*. Packet composition is data identifier (DI) byte, two bytes payload, and one ECC byte. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
11h	Generic Short Read Response, 1 byte returned	Short
12h	Generic Short Read Response, 2 bytes returned	Short

- ***Generic Long Read Response***

It is a long-packet response to *Generic READ Request*. Packet composition is DI byte, two bytes Word Count, ECC byte, N bytes of payload, and two bytes Checksum. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
1Ah	Generic Long Read response	Long

- ***DCS Long Read Response***

It is a long-packet response to *DCS Read Request*. Packet composition is DI byte, two bytes Word Count, ECC byte, N bytes payload, and two bytes Checksum. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
1Ch	DCS Long Read response	Long

- ***DCS Short Read Response***

It is a short-packet response to *DCS Read Request*. Packet composition is DI byte, two bytes payload, and ECC byte. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
21h	DCS Short Read Response, 1 byte returned	Short
22h	DCS Short Read Response, 2 bytes returned	Short

■ ***Acknowledge and Error Report***

It is sent in response to any command, or read, request, with BTA asserted when a reportable error is detected in the preceding, or earlier, transmission from the host processor.

Data type (hex)	Description	Packet size
02h	Acknowledge and Error Report	Short

■ ***Generic Short Read Response***

It is a short-packet response to *Generic READ Request*. Packet composition is data identifier (DI) byte, two bytes payload, and one ECC byte. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
11h	Generic Short Read Response, 1 byte returned	Short
12h	Generic Short Read Response, 2 bytes returned	Short

■ ***Generic Long Read Response***

It is a long-packet response to *Generic READ Request*. Packet composition is DI byte, two bytes Word Count, ECC byte, N bytes of payload, and two bytes Checksum. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
1Ah	Generic Long Read response	Long

■ ***DCS Long Read Response***

It is a long-packet response to *DCS Read Request*. Packet composition is DI byte, two bytes Word Count, ECC byte, N bytes payload, and two bytes Checksum. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

Data type (hex)	Description	Packet size
1Ch	DCS Long Read response	Long

■ ***DCS Short Read Response***

It is a short-packet response to *DCS Read Request*. Packet composition is DI byte, two bytes payload, and ECC byte. If this command itself is possibly corrupt due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent. Instead, the *Acknowledge and Error Report* packet shall be sent to notify the host.

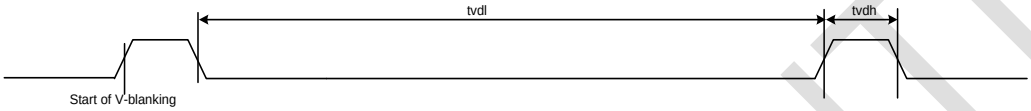
Data type (hex)	Description	Packet size
21h	DCS Short Read Response, 1 byte returned	Short
22h	DCS Short Read Response, 2 bytes returned	Short

5.4 Tearing Effect Output

A command mode display module has its own timing controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module. In a DSI system, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor when requested, using the bidirectional Data Lane. The PHY for DSI has no inherent interrupt capability from peripheral to host processor so the host processor shall either rely on polling, or it shall give bus ownership to the peripheral for extended periods.

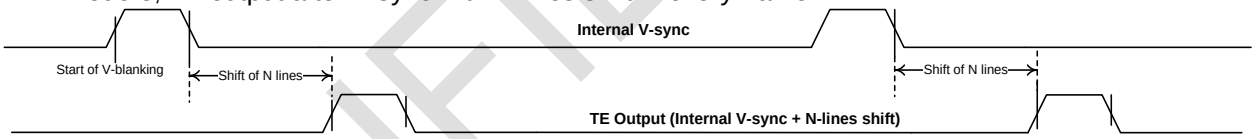
The function of TE-reporting from display module is enabled and disabled by the following DCS commands: set_tear_on(0x35h), set_tear_scanline(0x44), and set_tear_off(0x34h). Command set_tear_on and set_tear_scanline are sent to the display module as DSI data type 0x15 (DCS Short Write, one parameter) and DSI data type 0x39 (DCS Long Write/write_LUT), respectively. The TE output of different tearing effect modes are shown as follows:

- Mode 1, TE output consists of V-sync information only:



- Mode 2, TE output consists of both V-sync and H-sync information:

- Mode 3, TE output after V-sync with *N* lines shift in every frame:



Mode selection for TE output

TEON (0x35h)	TELOM(0x35h[0])	STESL(0x44h[15:0])	TE Output
Command is not set	X	X	GND
Command is set	0	X	TE (Mode 1)
Command is set	1	16’b0	TE (Mode 2)
Command is set	1	N	TE (Mode 3)

5.5 Picture Parameter Set (PPS)

5.5.1 Compression Mode Command, Data Type = 00 0111 (0x07)

Some display stream compression parameters may be configured using the Compression Mode Command, which is a short packet consisting of a DI byte, a two-byte payload and an ECC byte. This packet signals whether compression is enabled or disabled and the coding system used to create a bitstream or codestream that is carried by the Compressed Pixel Stream data type transaction. This data type writes the compression mode parameters listed in Table PPS setting to the peripheral in advance of the codestream with timing dependency.

Table PPS setting

SP Byte	Bit Location	Bit Description And Assigned Values
Data 0	7:6	Reserved, bits equal 0
Data 0	5:4	PPS selector 00 = PPS Table 1 (or no tables stored, default reset value) 01 = PPS Table 2 10 = PPS Table 3 11 = PPS Table 4
Data 0	3	Reserved
Data 0	2:1	Algorithm identifier 00 = VESA DSC Standard 1.1 11 = vendor-specific algorithm 01, 10 = reserved, not used
Data 0	0	0 = compression disabled (default) 1 = compression enabled
Data 1	7:0	Reserved, bits equal 0

The Command mode contains a two-bit PPS Selector that may be used to enable a pre-stored PPS Table for controlling the compression decoder parameters. The processor sends this data type to change the decoder parameters that shall take effect following the next vertical sync or internal vertical sync (if using command mode). The PPS Selector is an optional field; if no table is stored in the receiver, the selector shall be 00b.

5.5.2 Picture Parameter Set (0x0A)

The Picture Parameter Set (PPS) data type is a long packet used to transmit a pre-defined set of parameters that control a compression coding system. The packet shall consist of a DI byte, a two-byte, non-zero WC, an ECC byte, a payload containing WC bytes, and a two-byte checksum.
The size, content and timing context of this long packet is defined by the coding system designated in the Compression Mode data type,Compression Mode Command, and transported in the Compressed Image Format data type, Compressed Pixel Stream. Using this long packet, for example, may replace adding header markers to a bitstream.

If the peripheral receiver supports multiple, stored PPS tables, the received new PPS data is stored in the table designated by the Compression Mode PPS Selector if the table is writable.

5.5.3 Compressed Pixel Stream, Long Packet, Data Type = 00 1011 (0x0B)

The Compressed Pixel Stream is a long packet that carries compressed data to a Video Mode display module. This packet shall consist of a DI byte, a two-byte non-zero WC, an ECC byte, a payload containing WC bytes and a two-byte checksum, shown in Figure 30.

This is an optional packet, but if the pixel data is compressed, this packet shall carry the compressed image data when the Compression Mode packet (Compression Mode Command,) has signaled that compression is enabled.

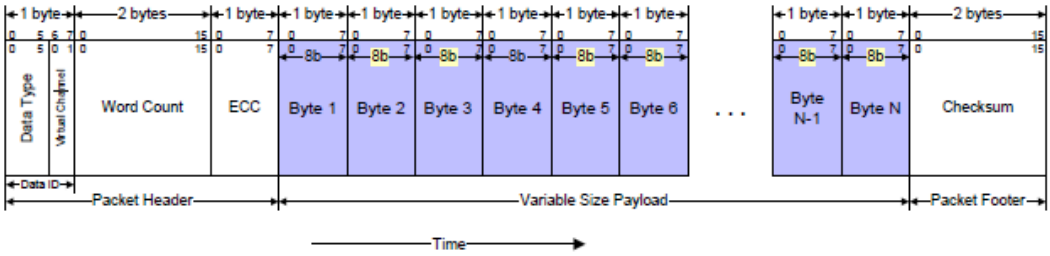
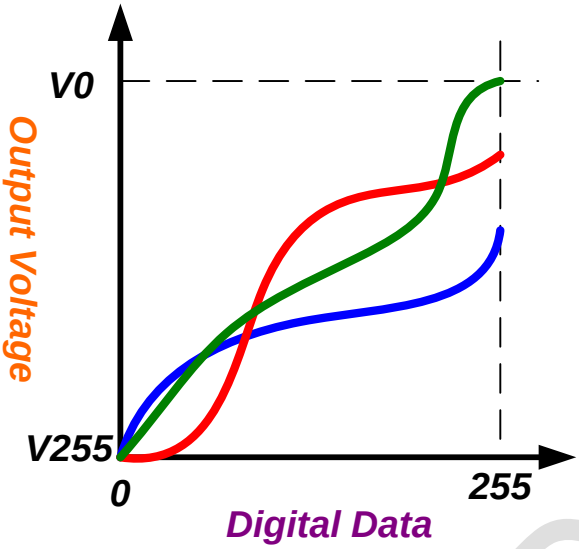


Figure 30 Compressed Pixel Stream Format, Long Packet

5.6 Digital 3-Gamma Adjustment

The RM69700 supports independent gamma adjustment function for R, G and B dots separately to display maximum 16.7M colors of one pixel. This function is implemented by selecting different grayscale levels incorporating with gamma adjustment settings. The driver's source outputs corresponding to different color dots are briefly depicted in the following figure. The relation between source outputs and color dots is set by the selection of color order on the panel.



6. Command

6.1 Command List

■ **User Command Set**

Instruction	Address		D7	D6	D5	D4	D3	D2	D1	D0	Default
	MIPI	Non-MIPI									
NOP	00h	0000h	No argument								N/A
SWRESET	01h	0100h	No argument								N/A
RDDID	04h	0400h	ID1[7:0]								00h
		0401h	ID2[7:0]								80h
		0402h	ID3[7:0]								00h
RDNUMED	05h	0500h	RDNUMED[7:0]								00h
RDDPM	0Ah	0A00h	BSTON	IDMON	-	SLPOUT	NORON	DISPON	-	-	08h
RDDMADCTL	0Bh	0B00h	-	-	-	-	RGB	-	RSMX	RSMY	00h
RDDCOLMOD	0Ch	0C00h	-	VIPF2	VIPF1	VIPF0	-	IFPF2	IFPF1	IFPF0	77h
RDDIM	0Dh	0D00h	-	-	INVON	ALLPON	ALLPOFF	0	0	0	00h
RDDSM	0Eh	0E00h	TEON	M	-	-	-	-	-	ERR	00h
RDDSDR	0Fh	0F00h	D7	D6	D5	D4	-	-	-	CMP_BIT	00h
SLPIN	10h	1000h	No argument								N/A
SLPOUT	11h	1100h	No argument								N/A
PARON	12h	1200h	No argument								N/A
NORON	13h	1300h	No argument								N/A
INVOFF	20h	2000h	No argument								N/A
INVON	21h	2100h	No argument								N/A
ALLPOFF	22h	2200h	No argument								N/A
ALLPON	23h	2300h	No argument								N/A
DISPOFF	28h	2800h	No argument								N/A
DISPON	29h	2900h	No argument								N/A
RAMWR	2Ch	2C00h	No argument								N/A
TEOFF	34h	3400h	No argument								N/A
TEON	35h	3500h	0	0	0	0	0	0	0	TELOM	00h
MADCTL	36h	3600h	0	0	0	0	RGB	0	RSMX	RESMY	00h
IDMOFF	38h	3800h	No argument								N/A
IDMON	39h	3900h	No argument								N/A
COLMOD	3Ah	3A00h	0	VIPF2	VIPF1	VIPF0	0	IFPF2	IFPF1	IFPF0	77h
RAMWRC	3Ch	3C00h	D7	D6	D5	D4	D3	D2	D1	D0	00h
STESL	44h	4400h	STS[15:8]								00h
		4401h	STS[7:0]								00h
GSL	45h	4500h	-	-	-	-	GTS[11:8]				00h
		4501h	GTS[7:0]								00h

DSTBON	4Fh	00h	0	0	0	0	0	0	0	DSTB	00h
WRDISBV	51h	5100h	DBV[7:0]								00h
		5101h	DBV[15:8]								00h
RDDISBV	52h	5200h	DBV[7:0]								00h
		5201h	DBV[15:8]								00h
WRHBMBC	53h	00h	HBM[1:0]		BC	0	DD	0	0	0	20h
RDHBMBC	54h	00h	HBM[1:0]		BC	-	DD	-	-	-	20h
WRRADACL	55h	00h	0	0	0	0	0	0	ACL[1:0]		00h
RDRADACL	56h	00h	-	-	-	-	-	-	ACL[1:0]		00h
WRCE	58h	00h	CTE_EN	CTE_LEVEL[3:0]				CTE_SLR_EN	0	0	48h
RDCE	59h	00h	CTE_EN	CTE_LEVEL[3:0]				CTE_SLR_EN	-	-	48h
WRCE1	5Ah	00h	SKIN_EN	0	SKIN_LEVEL[1:0]		EN_VIVID_ENH	0	CE_LEVEL[1:0]		11h
RDCE1	5Bh	00h	SKIN_EN	-	SKIN_LEVEL[1:0]		EN_VIVID_ENH	-	CE_LEVEL[1:0]		11h
WRCE2	5Ch	00h	SLR_EN	SLR_LEVEL[1:0]		EN_EDGE_ENH	EDGE_LEVEL[3:0]				24h
RDCE2	5Dh	00h	SLR_EN	SLR_LEVEL[1:0]		EN_EDGE_ENH	EDGE_LEVEL[3:0]				24h
WRCTS	62h	00h	TEMPER_EN	TEMPER_LEVEL[6:0]							00h
RDCTS	63h	00h	TEMPER_EN	TEMPER_LEVEL[6:0]							00h
WRPAPER	64h	00h	PER_EN	PAPER_LEVEL[6:0]							00h
RDPAPER	65h	00h	PER_EN	PAPER_LEVEL[6:0]							00h
WRWB	66h	00h	WB_EN	0	0	0	0	0	0	0	00h
RDWB	67h	00h	WB_EN	-	-	-	-	-	-	-	00h
RDDDBS	A1h	A100h	SID[15:8]								00h
		A101h	SID[7:0]								00h
		A102h	MID[15:8]								00h
		A103h	MID[7:0]								00h
		A104h	1	1	1	1	1	1	1	1	FFh
RDDDBC	A8h	A800h	SID[15:8]								00h
		A801h	SID[7:0]								00h
		A802h	MID[15:8]								00h
		A803h	MID[7:0]								00h
		A804h	1	1	1	1	1	1	1	1	FFh
RDFCS	AAh	00h	FCS[7:0]								00h
RDCCS	AFh	00h	CCS[7:0]								00h
SETDSIMODE	C2h	00h	-	-	-	-	RM	-	DM[1:0]		08h
RDID1	DAh	00h	ID1[7:0]								00h
RDID2	DBh	00h	ID2[7:0]								80h

RDID3	DCh	00h	ID3[7:0]	00h
WRCMDPAGE	FEh	00h	CMD_PG_SEL[7:0]	00h
RDCMDPAGE	FFh	00h	CMD_PG_SEL[7:0]	00h

■ Table of User Command Set

Instruction	Address		Status Availability			
	MIPI	Non-MIPI	Command(C) / Read (R) / Write (W)	Normal Mode On, Idle Mode Off, Sleep Out	Normal Mode On, Idle Mode On, Sleep Out	Sleep In
NOP	00h	0000h	C	Yes	Yes	Yes
SWRESET	01h	0100h	C	Yes	Yes	Yes
RDDID	04h	0400h	R	Yes	Yes	Yes
		0401h	R	Yes	Yes	Yes
		0402h	R	Yes	Yes	Yes
RDNUMED	05h	0500h	R	Yes	Yes	Yes
RDDPM	0Ah	0A00h	R	Yes	Yes	Yes
RDDMADCTL	0Bh	0B00h	R	Yes	Yes	Yes
RDDCOLMOD	0Ch	0C00h	R	Yes	Yes	Yes
RDDIM	0Dh	0D00h	R	Yes	Yes	Yes
RDDSM	0Eh	0E00h	R	Yes	Yes	Yes
RDDSDR	0Fh	0F00h	R	Yes	Yes	Yes
SLPIN	10h	1000h	C	Yes	Yes	Yes
SLPOUT	11h	1100h	C	Yes	Yes	Yes
PARON	12h	1200h	C	Yes	Yes	Yes
NORON	13h	1300h	C	Yes	Yes	Yes
INVOFF	20h	2000h	C	Yes	Yes	Yes
INVON	21h	2100h	C	Yes	Yes	Yes
ALLPOFF	22h	2200h	C	Yes	Yes	Yes
ALLPON	23h	2300h	C	Yes	Yes	Yes
DISPOFF	28h	2800h	C	Yes	Yes	Yes
DISPON	29h	2900h	C	Yes	Yes	Yes
RAMWR	2Ch	2C00h	W	Yes	Yes	Yes
TEOFF	34h	3400h	C	Yes	Yes	Yes
TEON	35h	3500h	W	Yes	Yes	Yes
MADCTL	36h	3600h	W	Yes	Yes	Yes
IDMOFF	38h	3800h	C	Yes	Yes	Yes
IDMON	39h	3900h	C	Yes	Yes	Yes
COLMOD	3Ah	3A00h	W	Yes	Yes	Yes
RAMWRC	3Ch	3C00h	W	Yes	Yes	Yes
STESL	44h	4400h	W	Yes	Yes	Yes
		4401h	W	Yes	Yes	Yes
GSL	45h	4500h	R	Yes	Yes	Yes
		4501h	R	Yes	Yes	Yes
DSTBON	4Fh	00h	W	Yes	Yes	Yes

WRDISBV	51h	5100h	W	Yes	Yes	Yes
		5101h	W	Yes	Yes	Yes
RDDISBV	52h	5200h	R	Yes	Yes	Yes
		5201h	R	Yes	Yes	Yes
WRHBMBC	53h	00h	W	Yes	Yes	Yes
RDHBMBC	54h	00h	R	Yes	Yes	Yes
WRRADACL	55h	00h	W	Yes	Yes	Yes
RDRADACL	56h	00h	R	Yes	Yes	Yes
WRCE	58h	00h	W	Yes	Yes	Yes
RDCE	59h	00h	R	Yes	Yes	Yes
WRCE1	5Ah	00h	W	Yes	Yes	Yes
RDCE1	5Bh	00h	R	Yes	Yes	Yes
WRCE2	5Ch	00h	W	Yes	Yes	Yes
RDCE2	5Dh	00h	R	Yes	Yes	Yes
WRCTS	62h	00h	W/R	Yes	Yes	Yes
RDCTS	63h	00h	R	Yes	Yes	Yes
WRPAPER	64h	00h	W/R	Yes	Yes	Yes
RDPAPER	65h	00h	R	Yes	Yes	Yes
WRWB	66h	00h	W/R	Yes	Yes	Yes
RDWB	67h	00h	R	Yes	Yes	Yes
RDDDBS	A1h	A100h	R	Yes	Yes	Yes
		A101h	R	Yes	Yes	Yes
		A102h	R	Yes	Yes	Yes
		A103h	R	Yes	Yes	Yes
		A104h	R	Yes	Yes	Yes
RDDDBC	A8h	A800h	R	Yes	Yes	Yes
		A801h	R	Yes	Yes	Yes
		A802h	R	Yes	Yes	Yes
		A803h	R	Yes	Yes	Yes
		A804h	R	Yes	Yes	Yes
RDFCS	AAh	00h	R	Yes	Yes	Yes
RDCCS	AFh	00h	R	Yes	Yes	Yes
SETDSIMODE	C2h	00h	W	Yes	Yes	Yes
RDID1	DAh	00h	R	Yes	Yes	Yes
RDID2	DBh	00h	R	Yes	Yes	Yes
RDID3	DCh	00h	R	Yes	Yes	Yes
WRCMDPAGE	FEh	00h	W	Yes	Yes	Yes
RDCMDPAGE	FFh	00h	R	Yes	Yes	Yes

MIPI Data Type

	Instruction Code	MIPI	03h Generic Short Write no para	13h Generic Short Write 1para	23h Generic Short Write 2para	29h Generic Long Write	04h Generic Read no para	14h Generic Read 1 para	24h Generic Read 2para	05h DCS Write no para	15h DCS Write 1 para	39h DCS Long Write	06h DCS Read no para
DCS	NOP	00h		YES	YES	YES				YES	YES	YES	
	SWRESET	01h		YES	YES	YES				YES	YES	YES	
	RDDID	04h						YES	YES				YES
	RDNUMED	05h						YES	YES				YES
	RDDPM	0Ah						YES	YES				YES
	RDDMADCTL	0Bh						YES	YES				YES
	RDDCOLMOD	0Ch						YES	YES				YES
	RDDIM	0Dh						YES	YES				YES
	RDDSM	0Eh						YES	YES				YES
	RDDSDR	0Fh						YES	YES				YES
	SLPIN	10h		YES	YES	YES				YES	YES	YES	
	SLPOUT	11h		YES	YES	YES				YES	YES	YES	
	PARON	12h		YES	YES	YES				YES	YES	YES	
	NORON	13h		YES	YES	YES				YES	YES	YES	
	INVOFF	20h		YES	YES	YES				YES	YES	YES	
	INVON	21h		YES	YES	YES				YES	YES	YES	
	ALLPOFF	22h		YES	YES	YES				YES	YES	YES	
	ALLPON	23h		YES	YES	YES				YES	YES	YES	
	DISPOFF	28h		YES	YES	YES				YES	YES	YES	
	DISPON	29h		YES	YES	YES				YES	YES	YES	
	RAMWR	2Ch		YES	YES	YES				YES	YES	YES	
	TEOFF	34h		YES	YES	YES				YES	YES	YES	
	TEON	35h		YES	YES	YES		YES	YES	YES	YES	YES	YES
	MADCTL	36h			YES	YES		YES	YES		YES	YES	YES
	IDMOFF	38h		YES	YES	YES				YES	YES	YES	
	IDMON	39h		YES	YES	YES				YES	YES	YES	
	COLMOD	3Ah			YES	YES		YES	YES		YES	YES	YES
	RAMWRC	3Ch			YES	YES					YES	YES	
	STESL	44h				YES		YES	YES			YES	YES
	GSL	45h						YES	YES				YES
	DSTBON	4Fh			YES	YES		YES	YES		YES	YES	YES
	WRDISBV	51h				YES		YES	YES			YES	YES
	RDDISBV	52h						YES	YES				YES
	WRHBMBC	53h			YES	YES		YES	YES		YES	YES	YES
	RDHBMBC	54h						YES	YES				YES
	WRRADACL	55h			YES	YES		YES	YES		YES	YES	YES
	RDRADACL	56h						YES	YES				YES
	WRCE	58h			YES	YES		YES	YES		YES	YES	YES
	RDCE	59h						YES	YES				YES
	WRCE1	5Ah			YES	YES		YES	YES		YES	YES	YES
	RDCE1	5Bh						YES	YES				YES
	WRCE2	5Ch			YES	YES		YES	YES		YES	YES	YES
	RDCE2	5Dh						YES	YES				YES
	WRCTS	62h			YES	YES		YES	YES		YES	YES	YES
	RDCTS	63h						YES	YES				YES
	WRPAPER	64h			YES	YES		YES	YES		YES	YES	YES
	RDPAPER	65h						YES	YES				YES
	WRWB	66h			YES	YES		YES	YES		YES	YES	YES
	RDWB	67h						YES	YES				YES
	RDDDBS	A1h						YES	YES				YES
	RDDDBC	A8h						YES	YES				YES
	RDFCS	AAh						YES	YES				YES

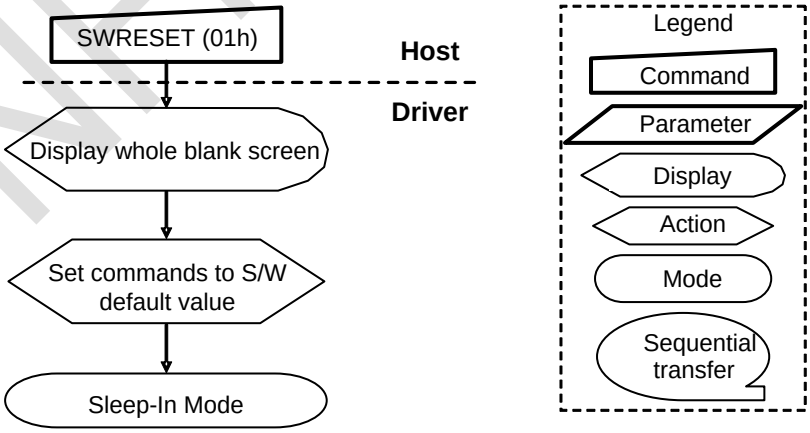
	RDCCS	AFh						YES	YES				YES
	SETDSIMODE	C2h			YES	YES		YES	YES		YES	YES	YES
	RDID1	DAh						YES	YES				YES
	RDID2	DBh						YES	YES				YES
	RDID3	DCh						YES	YES				YES
	WRCMDPAGE	FEh			YES	YES		YES	YES		YES	YES	YES
	RDCMDPAGE	FFh						YES	YES				YES
MCS	Page 0				YES	YES		YES	YES		YES	YES	YES
	Page 1				YES	YES		YES	YES		YES	YES	YES
	Page 2				YES	YES		YES	YES		YES	YES	YES
	Page 3				YES	YES		YES	YES		YES	YES	YES
	Page 4				YES	YES		YES	YES		YES	YES	YES
	Page 5				YES	YES		YES	YES		YES	YES	YES
	Page 6				YES	YES		YES	YES		YES	YES	YES
	Page 7				YES	YES		YES	YES		YES	YES	YES
	Page 8				YES	YES		YES	YES		YES	YES	YES

6.2 Command Description

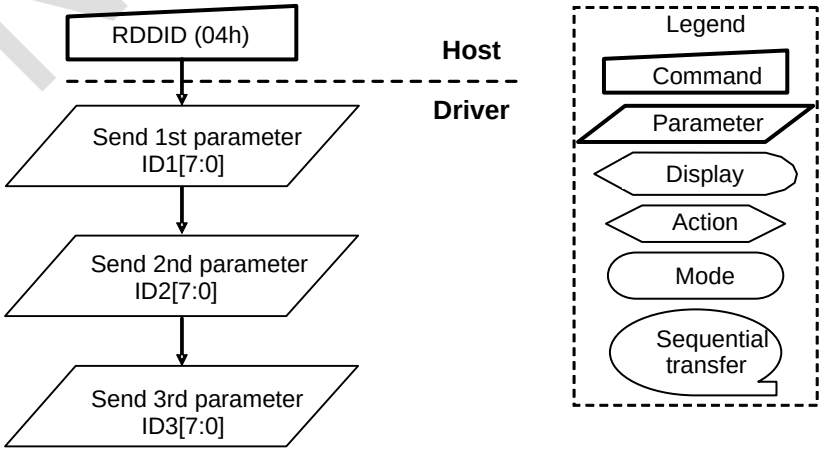
NOP (0000h): No Operation

<table>
<tr><th>0000H</th><th colspan="11">NOP</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="8">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>NOP</td><td>W</td><td>00h</td><td>0000h</td><td colspan="8">No Argument</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">This command is an empty command and has no effect on the display module.</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">None</td></tr>
</table>

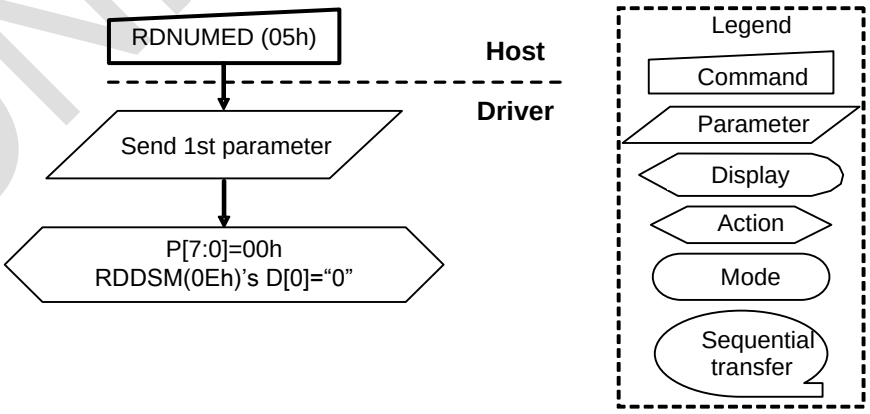
SWRESET (0100h): Software Reset

<table>
<tr><th>0100H</th><th colspan="11">SWRESET</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="8">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SWRESET</td><td>W</td><td>01h</td><td>0100h</td><td colspan="8">No Argument</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">When the Software Reset command is being executed, all related commands and parameters are reset to their S/W Reset default values.</td></tr>
<tr><td>Restriction</td><td colspan="12">Software reset command cannot be sent during Sleep-Out sequence. Any new command cannot be sent within 10-frame period until the device enters Sleep-In mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>N/A</td></tr>
<tr><td>SW Reset</td><td>N/A</td></tr>
<tr><td>HW Reset</td><td>N/A</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

RDDID (0400h): Read Display ID

<table>
<tr><th>0400H</th><th colspan="12">RDDID</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="3">RDDID</td><td rowspan="3">R</td><td rowspan="3">04h</td><td>0400h</td><td>-</td><td colspan="8">ID1[7:0]</td><td>00</td></tr>
<tr><td>0401h</td><td>-</td><td colspan="8">ID2[7:0]</td><td>80</td></tr>
<tr><td>0402h</td><td>-</td><td colspan="8">ID3[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">Command RDDID reads ID data. Its readout data is multiple parameters:
The 1st parameter ID1 is the module’s manufacture ID.
The 2nd parameter ID2 is the module/driver version ID.
The 3rd parameter ID3 is the module/driver ID</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>After OTP</th><th>Before OTP</th></tr>
<tr><td>Power On Sequence</td><td>OTP value</td><td>ID1=00h / ID2=80h / ID3=00h</td></tr>
<tr><td>SW Reset</td><td>OTP value</td><td>ID1=00h / ID2=80h / ID3=00h</td></tr>
<tr><td>HW Reset</td><td>OTP value</td><td>ID1=00h / ID2=80h / ID3=00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

RDNUMED (0500h): Read Number of Errors on DSI

<table>
<tr><th>0500H</th><th colspan="12">RDNUMED</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td>Address</td><td colspan="10">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>RDNUMED</td><td>R</td><td>05h</td><td>-</td><td>-</td><td colspan="8">P[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This read command is only applied to MIPI DSI interface and is of no function for other interfaces. The returned data is the recorded parity errors on DSI.
P[6:0] represents the number of parity errors.
P[7] is set to be “1” if there is overflow of P[6:0],
P[7:0] as well as RDDSM’s D[0] are reset to be “0”s after the read command is finished.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

RDDPM (0A00h): Read Display Power Mode

0A00H	RDDPM												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDPM	R	0Ah	0A00h	-	D7	D6	-	D4	D3	D2	-	-	08

Description

This command indicates the status of display driver's power and operation mode:

Bit	Symbol	Description	Comment
D7	BSTON	Boost Status	1 = Boost on, 0 = Boost off
D6	IDMON	Idle Mode On/Off	1 = Idle Mode On, 0 = Idle Mode Off
D4	SLPON	Sleep In/Out	1 = Sleep Out, 0 = Sleep In
D3	NORON	Display Normal Mode On/Off	1 = Normal Display, 0 = Partial Display
D2	DISPON	Display On/Off	1 = Display On, 0 = Display Off

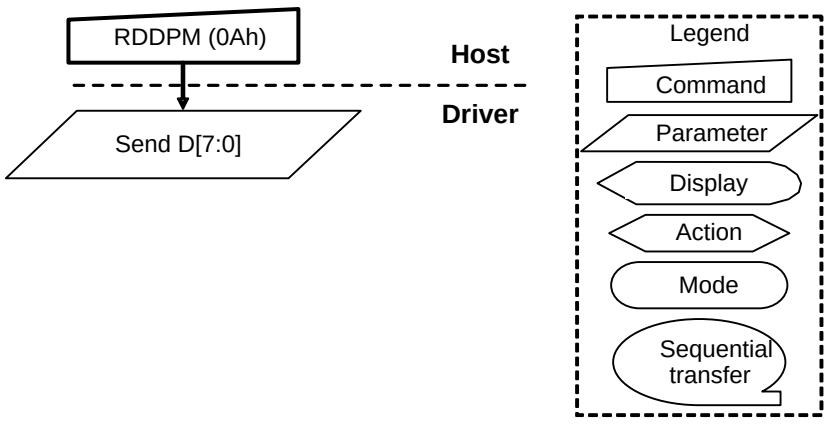
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
SW Reset	08h
HW Reset	08h

Flow Chart



RDDMADCTL (0B00h): Read Display MADCTL

0B00H	RDDMADCTL												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDMADCTL	R	0Bh	0B00h	-	-	-	0	-	D3	-	D1	D0	00

Description

This command indicates the current display status as described in the table below:

Bit	Symbol	Description	Comment
D7	Reserved	-	0
D6	Reserved	-	0
D4	Reserved	-	0
D3	RGB	Color order of sub-pixel	1 = BGR, 0 = RGB
D2	Reserved	-	0
D1	RSMX	Horizontal Flip	0 = Normal display 1 = Horizontal flip
D0	RSMY	Vertical Flip	0 = Normal display 1 = Vertical flip

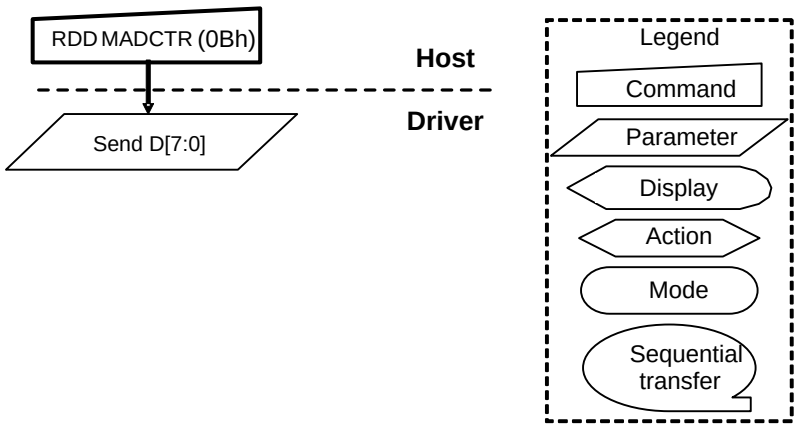
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDDCOLMOD (0C00h): Read Display Pixel Format

0C00H	RDDCOLMOD											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDCOLMOD	R	0Ch	0C00h	-	0	VIPF[2:0]			0	IFPF[2:0]			70

Description

This command indicates the current status of the display as described in the table below:

Bit	Symbol	Description	Comment
D6	VIPF[2]	DPI Pixel format (RGB interface color format)	3‘b101 = 16-bit / pixel, 3‘b110 = 18-bit / pixel, 3’b111 = 24-bit / pixel,
D5	VIPF[1]		
D4	VIPF[0]		
D2	IFPF[2]	DPI Pixel format (Control interface color format)	3‘b101 = 16-bit / pixel, 3‘b110 = 18-bit / pixel, 3’b111 = 24-bit / pixel,
D1	IFPF[1]		
D0	IFPF[0]		

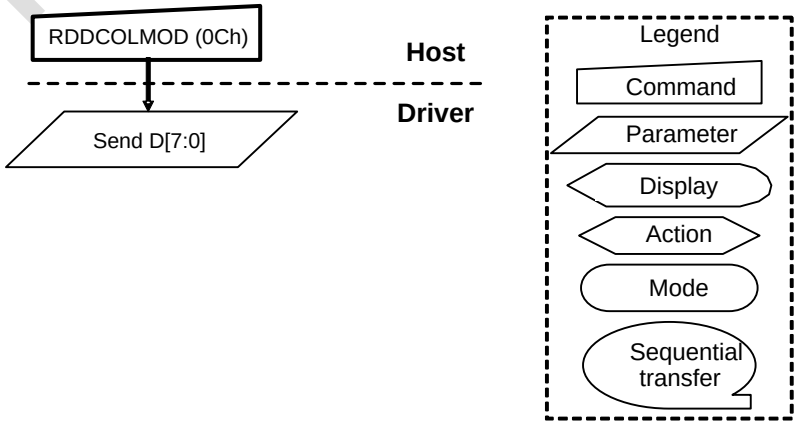
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	70h
SW Reset	70h
HW Reset	70h

Flow Chart



RDDIM (0D00h): Read Display Image Mode

0D00H	RDDIM												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDIM	R	0Dh	0D00h	-	0	0	D5	D4	D3	0	0	0	00

Description

The display module returns the display image mode status.

Bit	Symbol	Description	Comment
D5	INVON	Inversion On/Off	1 = Inversion is On, 0 = Inversion is Off
D4	ALLPON	All Pixel On	0 = Normal display 1 = White display (all-pixel on)
D3	ALLPOFF	All Pixel Off	0 = Normal display 1 = Black display (all-pixel off)

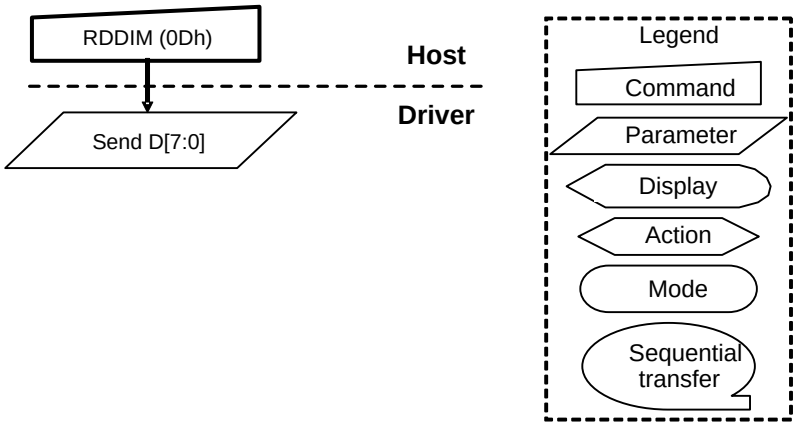
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDDSM (0E00h): Read Display Signal Mode

0E00H	RDDSM												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDSM	R	0Eh	0E00h	-	D7	D6	0	0	0	0	0	D0	00

Description

The display module returns the Display Signal Mode.

Bit	Symbol	Description	Comment
D7	TEON	Tearing effect line on/off	1 = On, 0 = Off
D6	M	Tearing effect line mode	0 = Mode-1, 1 = Mode-2
D0	Err	Error on DSI	0 = No Error, 1 = Error exists

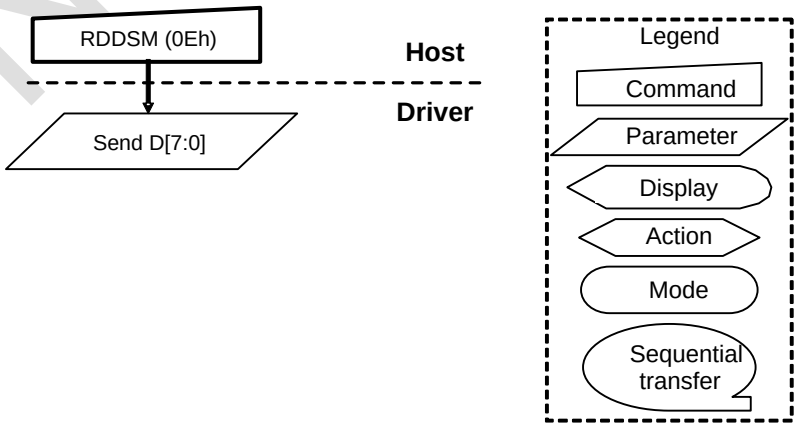
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



RDDSDR (0F00h): Read Display Self-Diagnostic Result

0F00H	RDDSDR												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDSDR	R	0Fh	0F00h	-	D7	D6	D5	D4	0	0	0	D0	00

Description

The display module returns the self-diagnostic results following a Sleep Out command.

Bit	Symbol	Description	Comment
D7	D7	Register loading check	Respond with SLPOUT command if check result are ok
D6	D6	Functionality check	
D5	D5	Chip attachment check	
D4	D4	Display glass break detect	
D0	CMP_BIT	Checksum Comparison	0 = Match, 1 = Not match

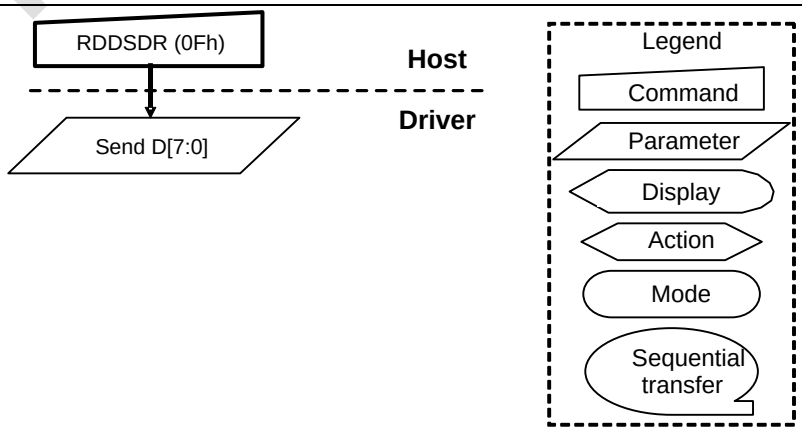
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



SLPIN (1000h): Sleep In

1000H	SLPIN											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
SLPIN	W	10h	1000h	No Argument									-
Description	This command forces display module to enter *Sleep-In* mode. Under this mode the DC/DC converter, internal display oscillator, and panel scanning are all stopped. The control interface and related registers are still working and keeps its values.												
Restriction	This command has no effect when the display driver is already in *Sleep-In* mode. SLPOUT command (11h) will force display driver to leave *Sleep-In* mode. It must wait at least 5msec to send the next command (for internal power and clock stabilization). And, it must wait 120msec after sending SLPOUT command for the next SLPIN command.												

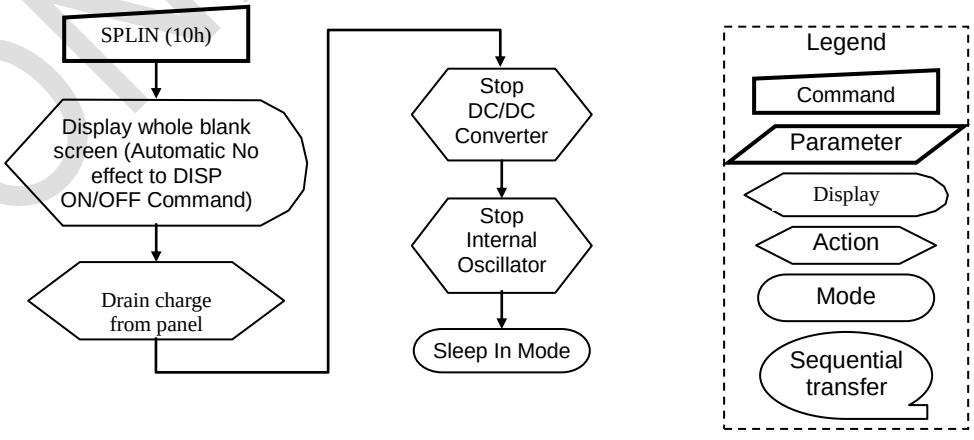
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart



SLPOUT (1100h): Sleep Out

1100H	SLPOUT											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
SLPOUT	W	11h	1100h	No Argument									-
Description	This command causes the display module to exit *Sleep-In* mode. All blocks inside display driver are enabled. The host needs to send PCLK, HS and VS information to display driver two frames before this command is sent when the display module is in *Normal* Mode.												
Restriction	This command shall not cause any visible effect on the display device when the display driver is not in *Sleep-In* mode. The host must wait 5msec after sending this command before any another commands. This delay allows internal power and clock circuits to be stabilized. After sending SLPOUT command, the host must wait 120 msec before sending SLPIN command.												

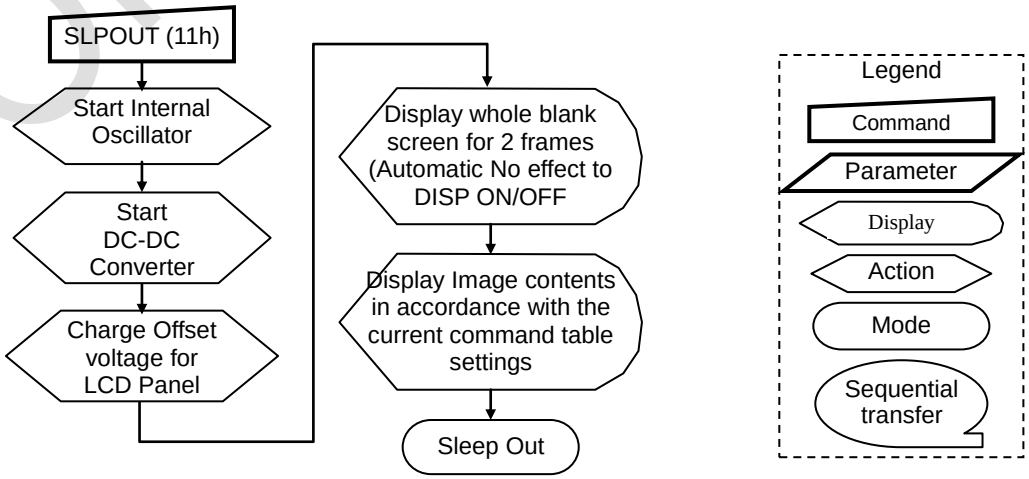
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

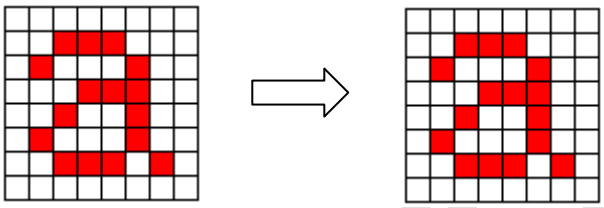
Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow chart



INVOFF (2000H): Exit Invert Mode

2000H	INVOFF											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
INVOFF	W	20h	2000h	No Argument									-
Description	This command causes the display module to stop inverting the image data on the display device. No status bits are changed. Input Image → Display Panel 												
Restriction	This command has no effect when module is already in inversion on mode.												

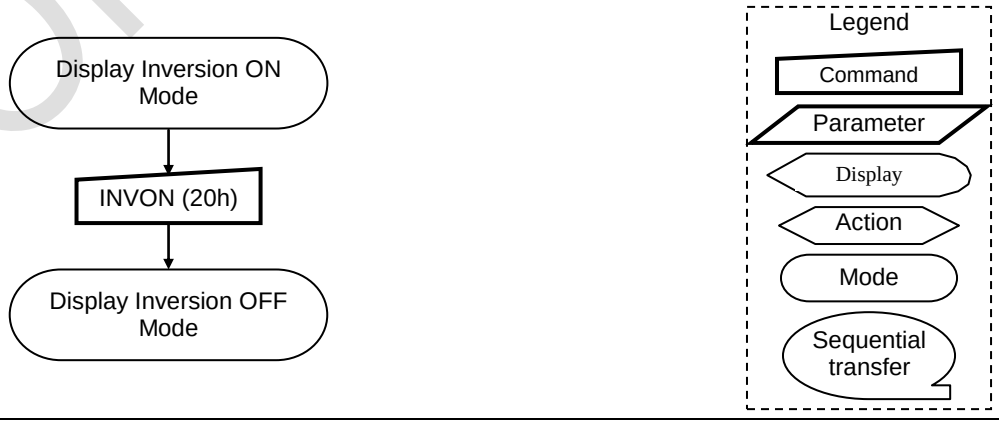
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

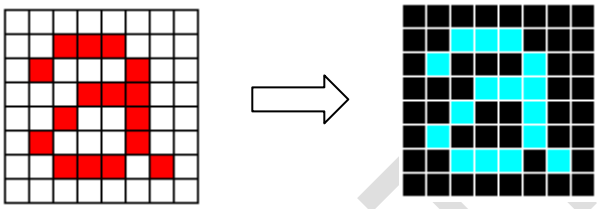
Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart



INVON (2100H): Enter Invert Mode

2100H	INVON											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
INVON	W	21h	2100h	No Argument									-
Description	This command causes the display module to invert the image data only on the display device. No status bits are changed. Input Image → Display Panel 												
Restriction	This command has no effect when module is already in inversion on mode.												

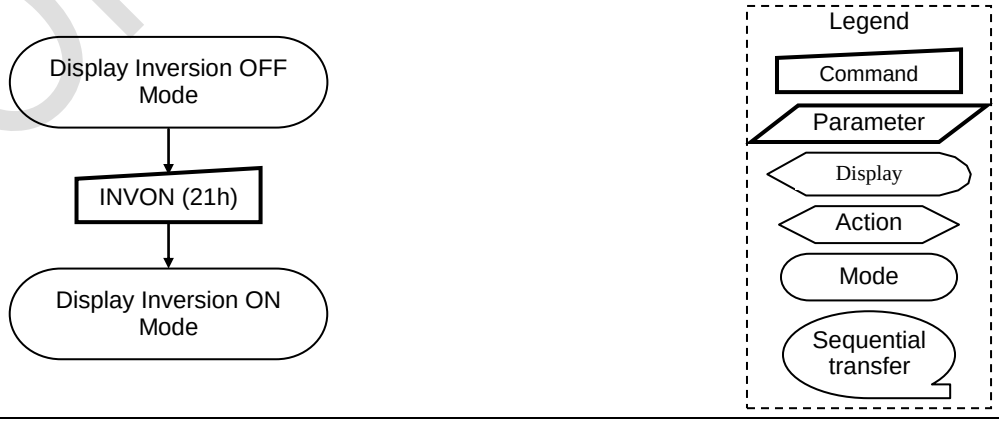
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

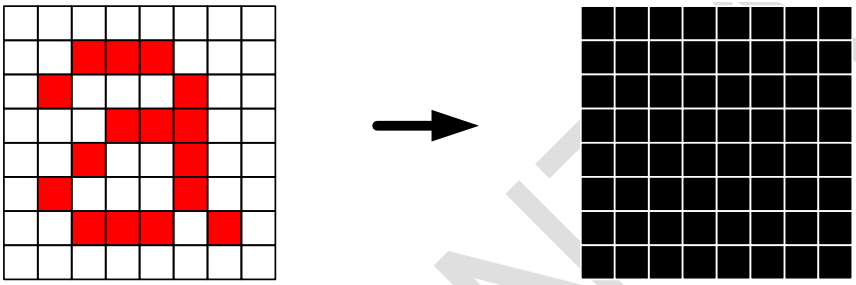
Default

Status	Default Value
Power On Sequence	Display Inversion off
SW Reset	Display Inversion off
HW Reset	Display Inversion off

Flow Chart



ALLPOFF (2200h): All Pixel Off

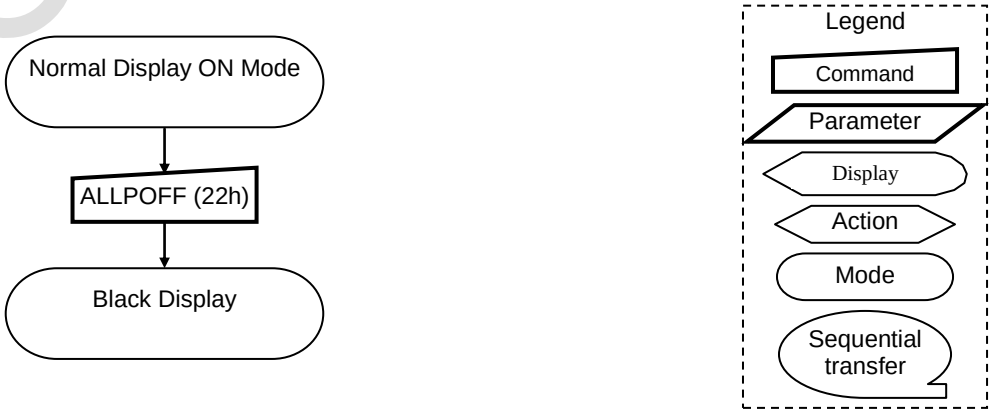
2200H	ALLPOFF											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
ALLPOFF	W	22h	2200h	No Argument									-
Description	This command turns the display panel black in Display On mode and a status of the Display On/Off register can be on or off. This command does not change any other status. **Input Image** → **Display Panel** 												
Restriction	-												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

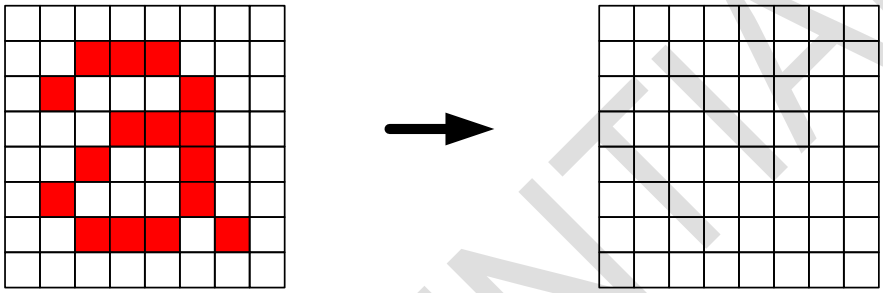
Default

Status	Default Value
Power On Sequence	All pixel Off is off
SW Reset	All pixel off is off
HW Reset	All pixel off is off

Flow Chart



ALLPON (2300h): All Pixel On

2300H	ALLPON											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
ALLPON	W	23h	2300h	No Argument									-
Description	This command turns the display panel white in Display On mode and a status of the Display On/Off register can be on or off. This command does not change any other status. **Input Image** → **Panel Display** 												
Restriction	-												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel on is off
SW Reset	All pixel on is off
HW Reset	All pixel on is off

Flow Chart

DISPOFF (2800h): Set Display Off

2800H	DISPOFF											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
DISPOFF	W	28h	2800h	No Argument									-
Description	This command causes the display module to stop displaying the image data on the display device. No status bits are changed.												
Restriction	This command has no effect when module is already in display off mode.												

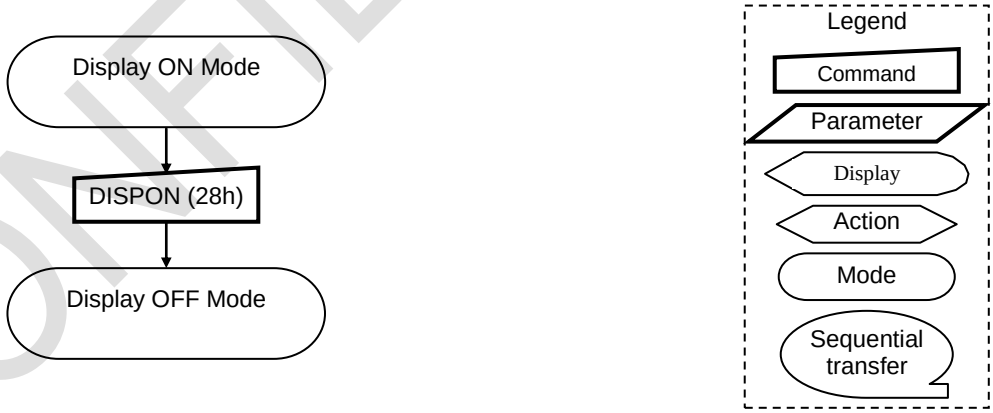
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart



DISPON (2900h): Set Display On

2900H	DISPON											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
DISPON	W	29h	2900h	No Argument									-
Description	This command causes the display module to start displaying the image data on the display device. No status bits are changed.												
Restriction	This command has no effect when module is already in display on mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart

RAMWR (2C00h): Memory Write

2C00H	RAMWR												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RAMWR	W	2Ch	2C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	--
	W	2Ch	2C01h	00h	D7	D6	D5	D4	D3	D2	D1	D0	--
	W	2Ch	2C02h	00h	D7	D6	D5	D4	D3	D2	D1	D0	--
Description	1. This command writes display data from the host to the on-chip memory buffer. 2. When this command is accepted, the address of memory buffer is reset to its start position and then sequential data are write to memory byte by byte until a full frame display data are write to the memory.												
Restriction	1. Sending any command can stop frame memory write. 2. For resolution of H= 1440RGB: - Without VESA DSC, the parameter size= 1440RGBx N (N is a multiple of 4) - With VESA DSC, the parameter size= 480RGBx N (N is a multiple of 4)												

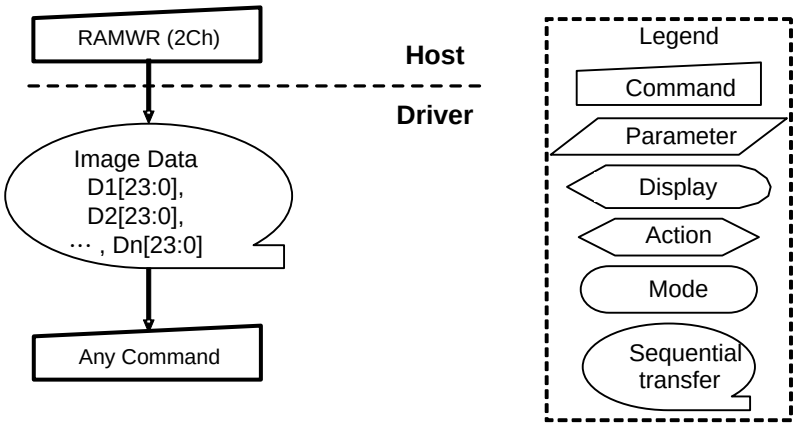
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart



TEOFF (3400h): Tearing Effect Line OFF

3400H	TEOFF											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
TEOFF	W	34h	3400h	No Argument									-
Description	This command stops outputting *Tearing Effect* output signal to pad.												
Restriction	This command has no effect when the *Tearing Effect* output is already off.												

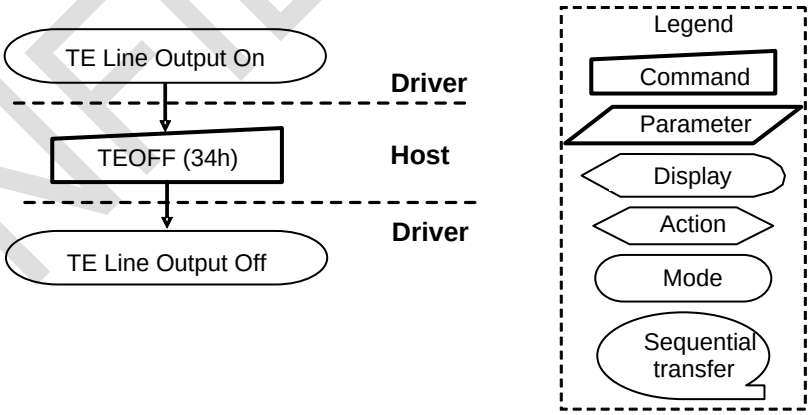
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



TEON (3500h): Tearing Effect Line ON

3500H	TEON											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
TEON	W	35h	3500h	00h	0	0	0	0	0	0	0	TELOM	00
Description	This command turns on the tearing effect output signal to the TE pad. The “Tearing Effect Line On” has one parameter that selects its output mode.												
Restriction	The tearing effect output is low if display module is under sleep mode.												

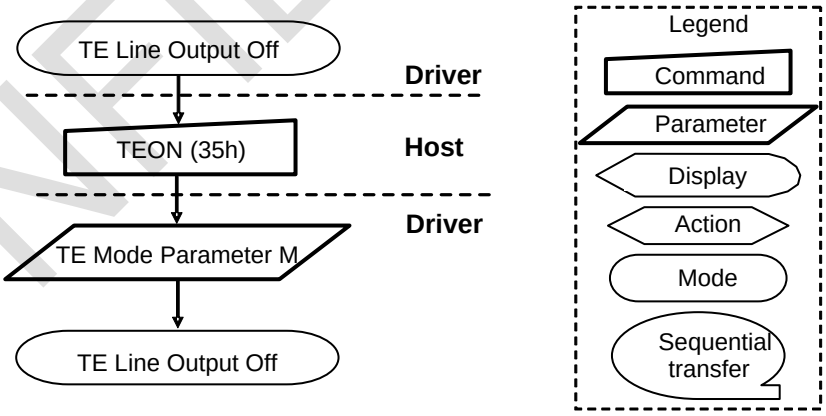
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	TE OFF
SW Reset	TE OFF
HW Reset	TE OFF

Flow Chart



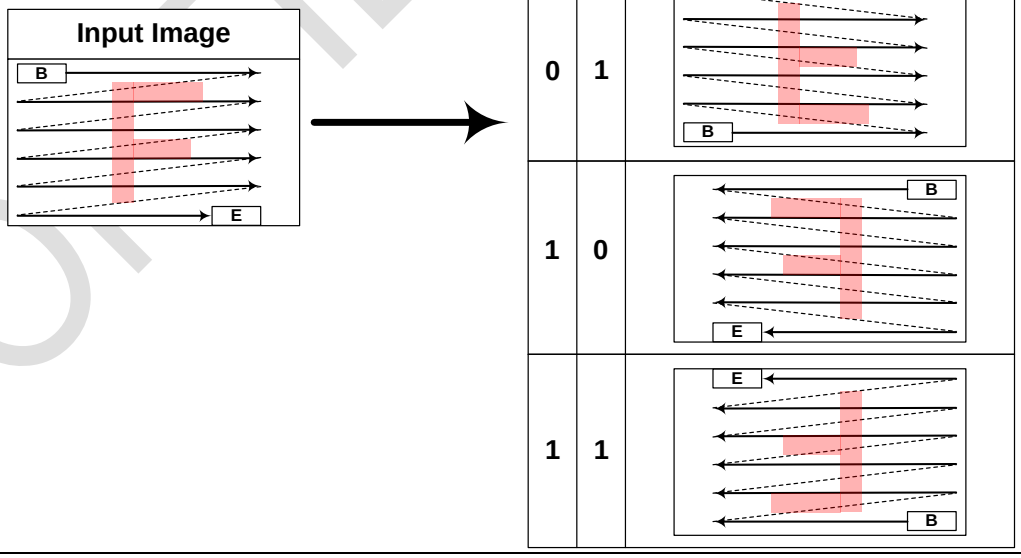
MADCTL (3600h): Memory Data Access Control

3600H	MADCTL											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
MADCTL	W	36h	3600h	00h	0	0	0	0	D3	0	D1	D0	00

Description

This command sets the scan direction of source and gate driver. This command makes no change on the other driver status.

Bit	Symbol	Description	Comment
D3	RGB	RGB/BGR Order	1 = BGR, 0 = RGB
D1	RSMX	Horizontal Flip	0 = Normal display 1 = Horizontal flip
D0	RSMY	Vertical Flip	0 = Normal display 1 = Vertical flip



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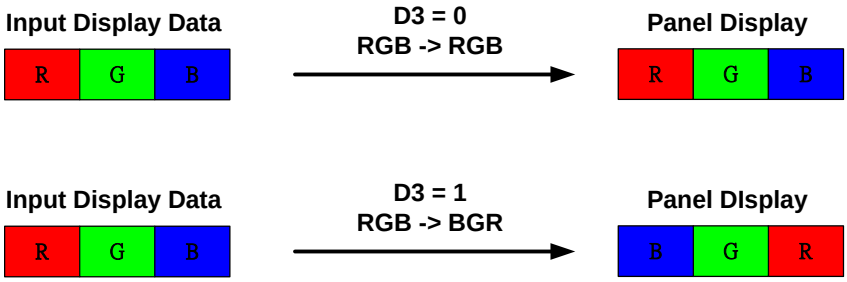
<tr><td></td><td> 
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<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
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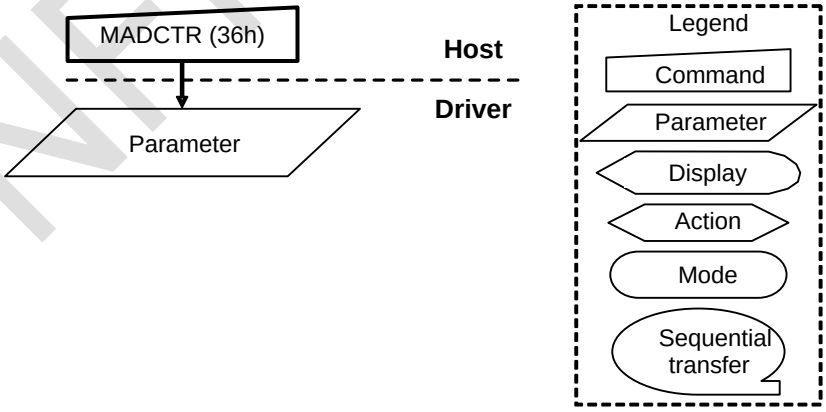
<tr><td>Flow chart</td><td> 
</td></tr>
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IDMOFF (3800h): Exit Idle Mode

3800H	IDMOFF											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
IDMOFF	W	38h	3800h	No Argument									-
Description	This command causes the display module to exit Idle mode.												
Restriction	This command has no effect when the display module is not in Idle mode.												

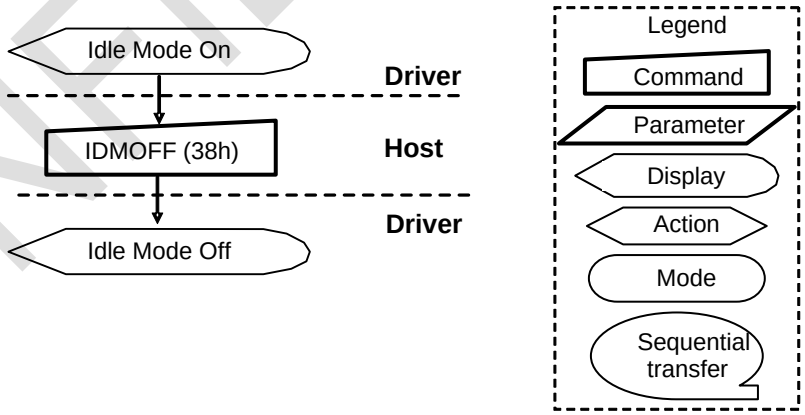
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart

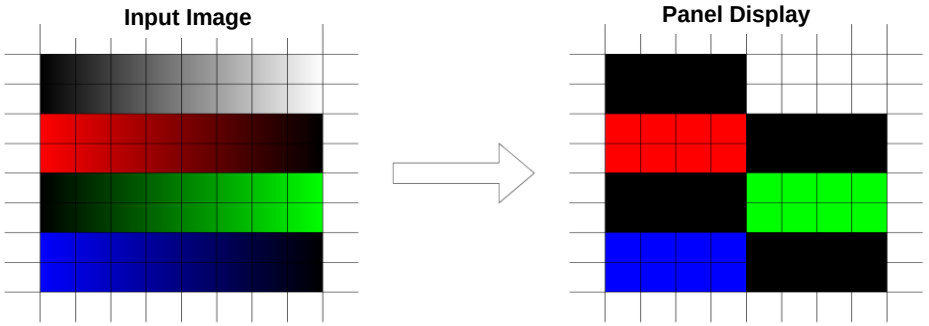


IDMON (3900h): Enter Idle Mode

3900H	IDMON											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
IDMON	W	39h	3900h	No Argument									-

Description

This command causes the display module to enter Idle Mode. After entering idle mode, color expression is reduced. Display device uses the MSB of input display data as the display data for each dot.



R[7:0]	G[7:0]	B[7:0]	Display Color on Panel
0XXXXXXX	0XXXXXXX	0XXXXXXX	Black
0XXXXXXX	0XXXXXXX	1XXXXXXX	Blue
1XXXXXXX	0XXXXXXX	0XXXXXXX	Red
1XXXXXXX	0XXXXXXX	1XXXXXXX	Magenta
0XXXXXXX	1XXXXXXX	0XXXXXXX	Green
0XXXXXXX	1XXXXXXX	1XXXXXXX	Cyan
1XXXXXXX	1XXXXXXX	0XXXXXXX	Yellow
1XXXXXXX	1XXXXXXX	1XXXXXXX	White

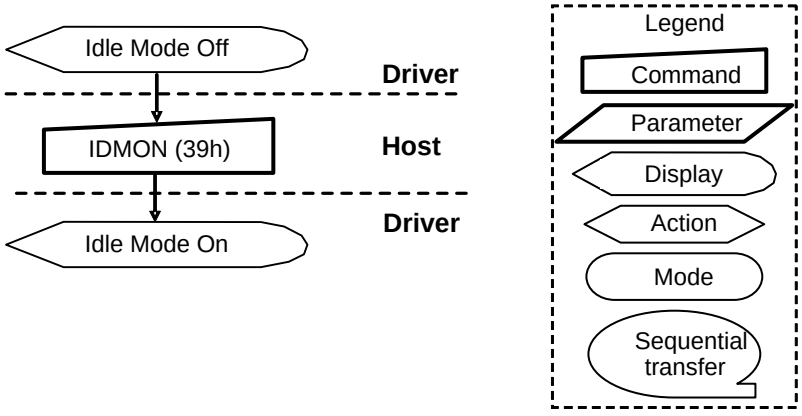
Restriction

This command has no effect when module is already in idle on mode.

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



COLMOD (3A00h): Interface Pixel Format

3A00H	COLMOD											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	W	3Ah	3A00h	00h	0	VIPF[2:0]			0	IFPF[2:0]			77

Description

This command is used to define the format of RGB input data.

Bit	Symbol	Description	Comment
D6	VIPF[2]	DPI Pixel format (RGB interface color format)	3‘b101 = 16-bit / pixel, 3‘b110 = 18-bit / pixel, 3’b111 = 24-bit / pixel,
D5	VIPF[1]		
D4	VIPF[0]		
D2	IFPF[2]	DPI Pixel format (Control interface color format)	3‘b101 = 16-bit / pixel, 3‘b110 = 18-bit / pixel, 3’b111 = 24-bit / pixel,
D1	IFPF[1]		
D0	IFPF[0]		

Restriction

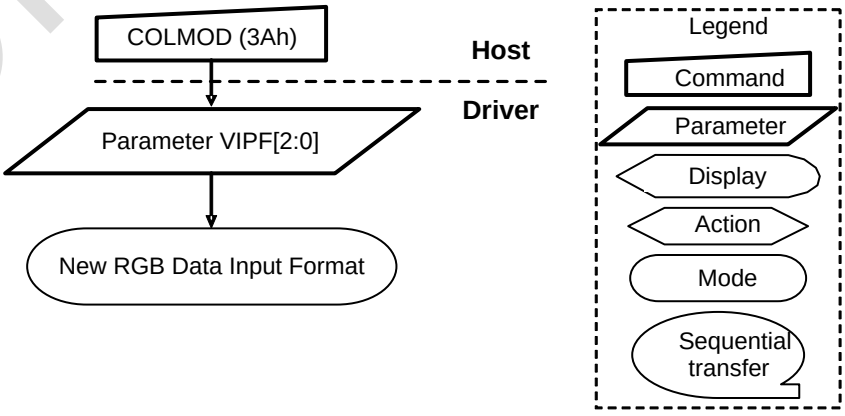
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

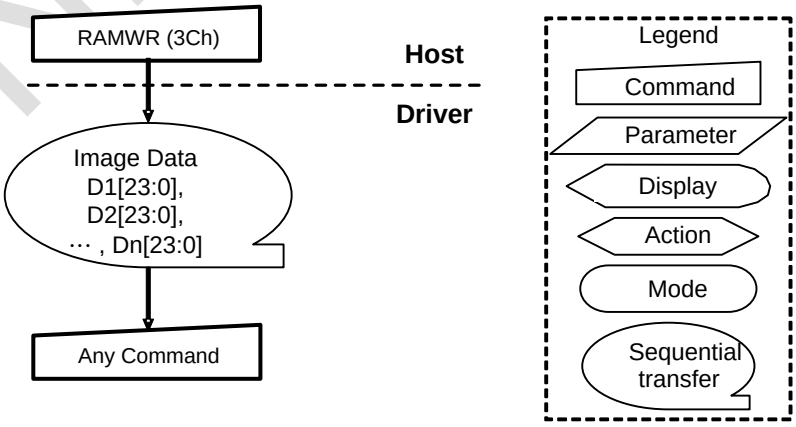
Default

Status	Default Value
Power On Sequence	70h
SW Reset	70h
HW Reset	70h

Flow Chart



RAMWRC (3C00h): Memory Write Continue

3C00H	RAMWRC											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RAMWRC	W	3Ch	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	--
	W	3Ch	3C01h	00h	D7	D6	D5	D4	D3	D2	D1	D0	--
	W	3Ch	3C02h	00h	D7	D6	D5	D4	D3	D2	D1	D0	--
Description	This command is used to continuously write the display data to the memory buffer following the RAMWR (0x2C) command.												
Restriction	1. For resolution of H= 1440RGB: - Without VESA DSC, the parameter size= 1440RGBx N (N is a multiple of 4) - With VESA DSC, the parameter size= 480RGBx N (N is a multiple of 4)												
Register Availability													
Default													
Flow Chart													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

STESL(4400h): Set Tear Scan Line

4400H	STESL											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
STESL	W	44h	4400h	00h	STS[15:8]								00
			4401h	00h	STS[7:0]								00
Description	This command turns on the display *Tearing Effect* output to the TE pad when the display line reaches N, set by STS[15:0].												
Restriction	The tearing effect output is active low when the display module is under sleep-in mode												

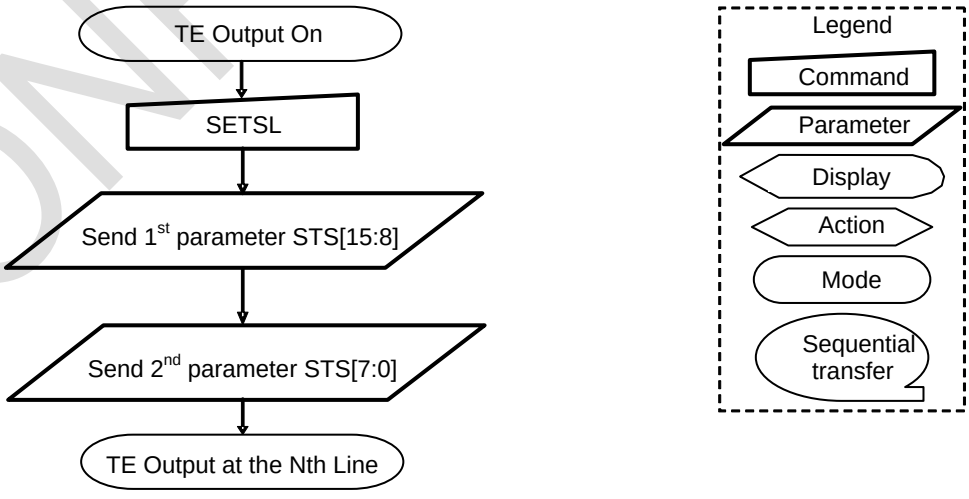
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS[15:0]=16'h0000
SW Reset	STS[15:0]=16'h0000
HW Reset	STS[15:0]=16'h0000

Flow Chart



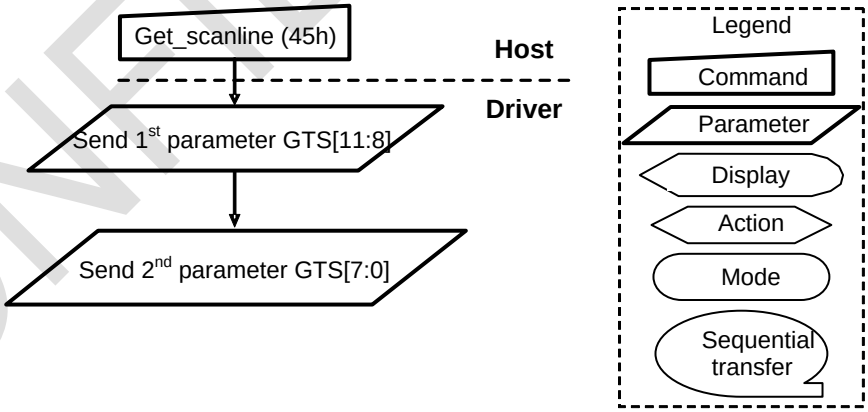
GSL (4500h): Get Scan Line

4500H	GSL											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
GSL	R	45h	4500h	-	-	-	-	-	GTS[11:8]				00
			4501h	-	GTS[7:0]								00
Description	The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When display module is under Sleep-In, the value of returned GTS[11:0] is undefined.											
Restriction	-											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Flow Chart



DSTBON (4F00h): Deep Standby Mode On

4F00H	DSTBON											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
DSTBON	W	4Fh	4F00h	00h	0	0	0	0	0	0	0	DSTB	00
Description	This command is used to force the display module to enter the deep standby mode. Pull RESX to low more than 3ms will force display driver to exit deep standby mode and revert to standby mode.												
Restriction													

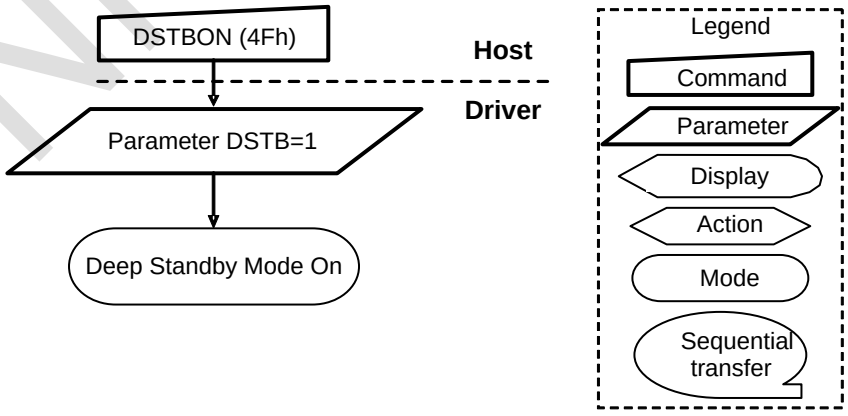
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



WRDISBV (5100h): Write Display Brightness

5100H	WRDISBV											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRDISBV	W	51h	5100h	00h	DBV[7:0]								00
			5101h	00h	DBV[15:8]								00
Description	This command is used to adjust brightness value.												
Restriction	The display supplier cannot use this command for tuning												

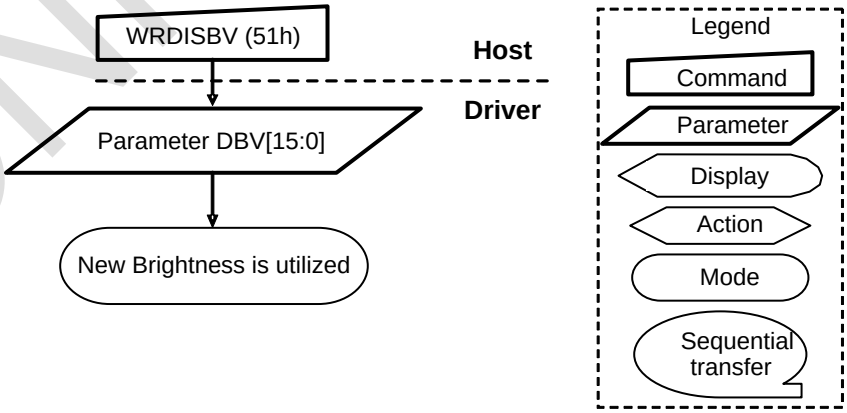
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDDISBV (5200h): Read Display Brightness

5200H	RDDISBV											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDISBV	R	52h	5200h	-	DBV[7:0]								00
			5201h	-	DBV[15:8]								00
Description	8bit : 5100[7:0] 10bit : 5100[1:0], 5101[7:0] 12bit : 5100[3:0], 5101[7:0]												
Restriction	-												

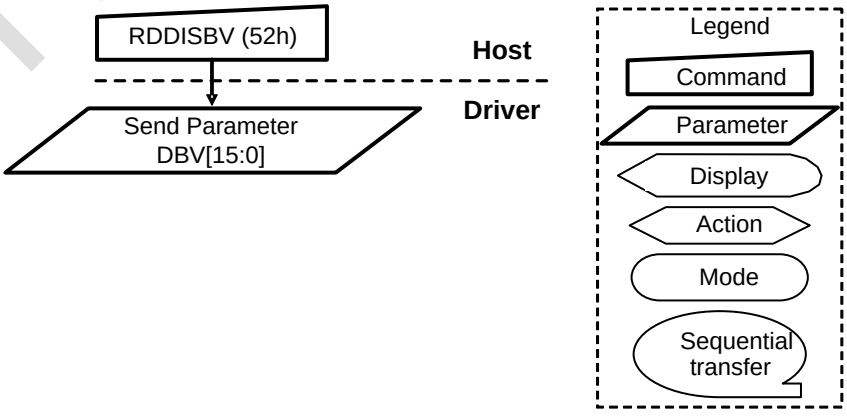
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRHBMBC (5300h): Select HBM and Enable BC Control

5300H	WRHBMBC											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRHBMBC	R/W	53h	5300h	00h	HBM[1:0]		BC	0	DD	0	0	0	20

Description

This command sets the selection of HBM mode and the control bit of brightness and dimming.

Bit	Symbol	DESCRIPTION	Comment
D[7:6]	HBM[1:0]	Selection of high brightness mode	HBM = 2'b11, HBM level 3 HBM = 2'b10, HBM level 2 HBM = 2'b01, HBM level 1 HBM = 2'b00, HBM mode is disable
D5	BC	Brightness control	BC = 0, Brightness control is off BC = 1, Brightness control is on
D3	DD	Backlight dimming enable control	DD = 0, Display dimming is off DD = 1, Display dimming is on

Restriction

The display supplier cannot use this command for tuning

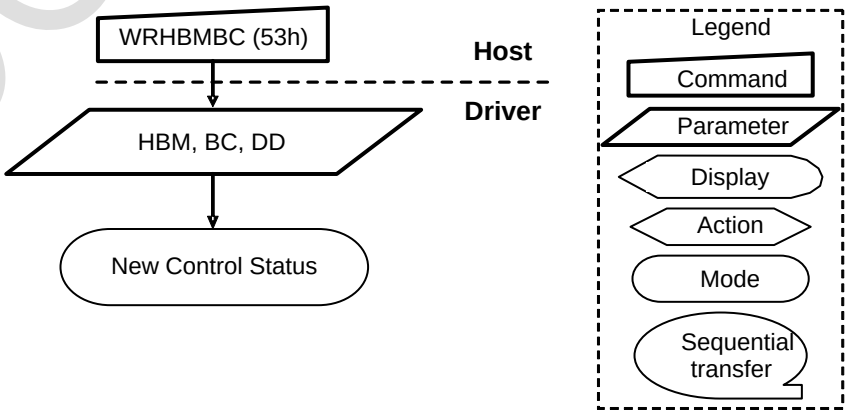
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	20h
SW Reset	20h
HW Reset	20h

Flow chart



RDHBMBC (5400h): Read HBM and BC Control

5400H	RDHBMBC											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRHBMBC	R	54h	5400h	-	HBM[1:0]		BC	0	DD	0	0	0	20

Description

This command reads the status of backlight output control.

Bit	Symbol	DESCRIPTION	Comment
D[7:6]	HBM[1:0]	Selection of high brightness mode	HBM = 2'b11, HBM level 3 HBM = 2'b10, HBM level 2 HBM = 2'b01, HBM level 1 HBM = 2'b00, HBM mode is disable
D5	BC	Brightness control	BC = 0, Brightness control is off BC = 1, Brightness control is on
D3	DD	Backlight dimming enable control	DD = 0, Display dimming is off DD = 1, Display dimming is on

Restriction

The display supplier cannot use this command for tuning

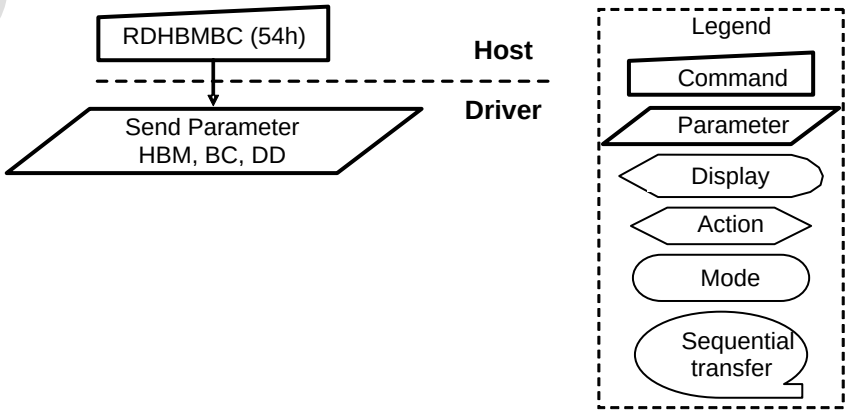
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	20h
SW Reset	20h
HW Reset	20h

Flow Chart



WRRADACL (5500h): Write RAD_ACL Control

5500h	WRRADACL											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1 D0	
WRRADACL	R/W	55h	5500h	00h	0	0	0	0	0	0	ACL[1:0]	00

Description

This command is used to set the control and level of ACL mode

Bit	Symbol	DESCRIPTION	Comment
D[1:0]	ACL[1:0]	Selection of Auto-Current Limit level	ACL = 2'b11, ACL effect is high ACL = 2'b10, ACL effect is medium ACL = 2'b01, ACL effect is low ACL = 2'b00, ACL function is disable

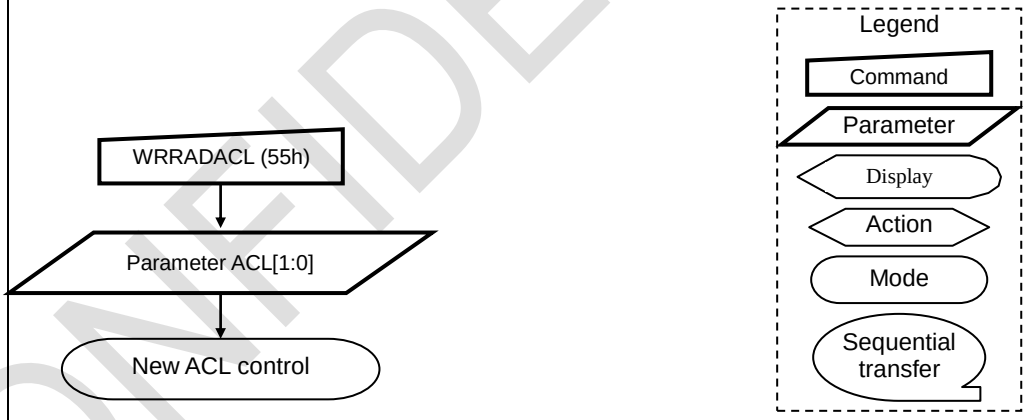
Restriction

-

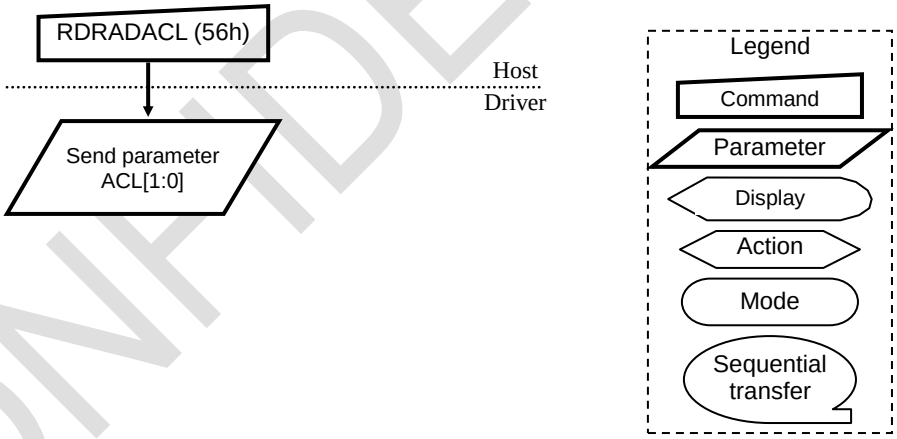
Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDRADACL (5600h): Read RAD_ACL Control

<table>
<tr><th>5600h</th><th colspan="12">RDRADACL</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>RDRADACL</td><td>R</td><td>56h</td><td>5600h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td colspan="2">ACL1:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to read the status of ACL mode
<table>
<tr><td>Bit</td><td>Symbol</td><td>DESCRIPTION</td><td>Note</td></tr>
<tr><td>D[1:0]</td><td>ACL[1:0]</td><td>Selection of
Auto-Current Limit level</td><td>ACL = 2’b11, ACL effect is high
ACL = 2’b10, ACL effect is medium
ACL = 2’b01, ACL effect is low
ACL = 2’b00, ACL function is disable</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

WRCE (5800h): Write Color Enhancement Control

5800H	8WRCE											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRCE	R/W	58h	5800h	00h	C7	C6	C5	C4	C3	C2	0	0	48

Description

This command is used to set parameters for contrast enhancement mode.

Bit	Symbol	Description	Comment
C7	CTE_EN	Contrast Enhancement Enable	0 : CTE function disable 1 : CTE function enable
C6 ~ C3	CTE_LEVEL[3:0]	CTE level selection	
C2	Reserved	-	Reserved

Restriction

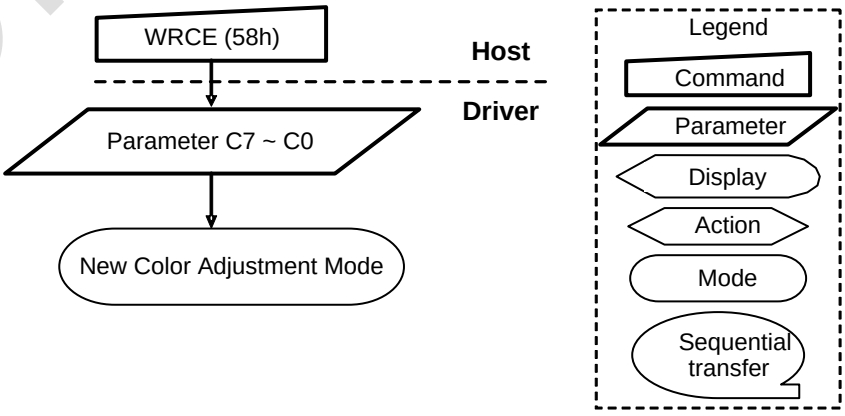
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	48h
SW Reset	48h
HW Reset	48h

Flow chart



RDCE (5900h): Read Color Enhancement Control

5900H	RDCE											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDCE	R	59h	5900h	-	C7	C6	C5	C4	C3	0	C1	C0	48

Description

This command is used to read parameters for contrast enhancement mode.

Bit	Symbol	Description	Comment
C7	CTE_EN	Contrast Enhancement Enable	0 : CTE function disable 1 : CTE function enable
C6 ~ C3	CTE_LEVEL[3:0]	CTE level selection	
C2	Reserved	-	Reserved

Restriction

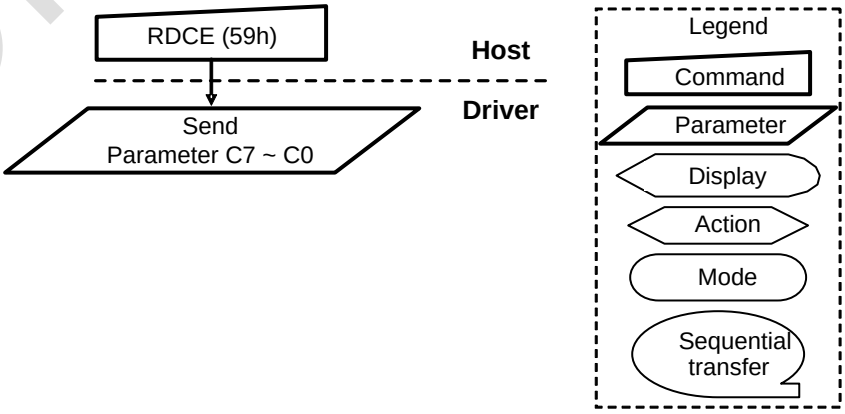
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	48h
SW Reset	48h
HW Reset	48h

Flow Chart



WRCE1 (5A00h): Write CE1

5A00H	WRCE												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRCE1	R/W	5Ah	5A00h	00h	C7	0	C5	C4	C3	0	C1	C0	11

Description

This command is used to set parameters for skin tone and vivid color mode.

Bit	Symbol	Description	Comment
C7	SKIN_EN	Skin Color enable	0 : Skin tone compensation off 1 : Skin-tone compensation on
C[5:4]	SKIN_LEVEL[1:0]	Skin Color level	
C3	EN_VIVID_ENH	Vivid Color enable	0 : Vivid color mode off 1 : Vivid color mode on
C[1:0]	CE_LEVEL[1:0]	Vivid Color Level	

Restriction

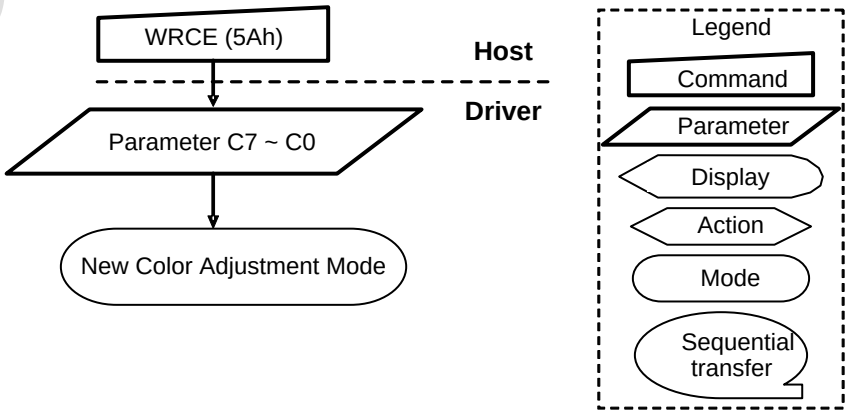
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	11h
SW Reset	11h
HW Reset	11h

Flow chart



RDCE1 (5B00h): Read Color Enhancement Control

5B00H	RDCE											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDCE1	R	5Bh	5B00h	-	C7	0	C5	C4	C3	0	C1	C0	11

Description

This command is used to read parameters of skin tone and vivid color mode.

Bit	Symbol	Description	Comment
C7	SKIN_EN	Skin Color enable	0 : Skin tone compensation off 1 : Skin-tone compensation on
C[5:4]	SKIN_LEVEL[1:0]	Skin Color level	
C3	EN_VIVID_ENH	Vivid Color enable	0 : Vivid color mode off 1 : Vivid color mode on
C[1:0]	CE_LEVEL[1:0]	Vivid Color Level	

Restriction

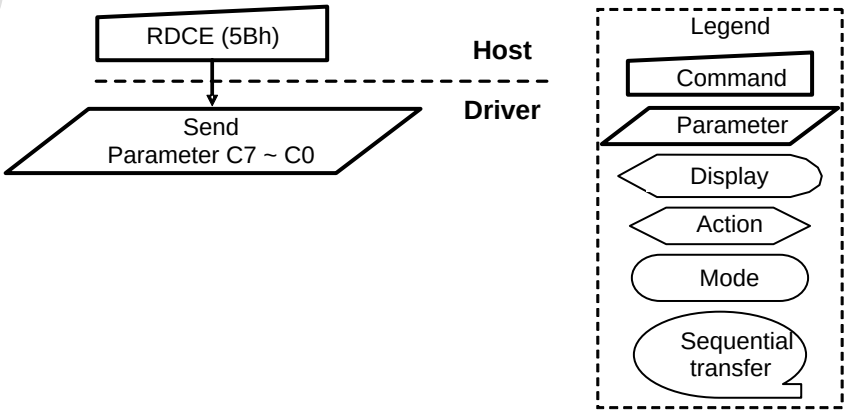
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

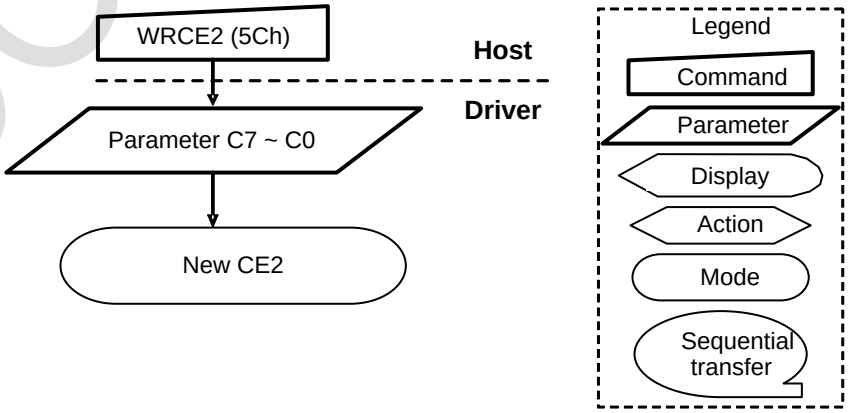
Default

Status	Default Value
Power On Sequence	11h
SW Reset	11h
HW Reset	11h

Flow Chart



WRCE2 (5C00h): Write CE2

<table>
<tr><th>5C00h</th><th colspan="13">WRCE2</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>WRCE2</td><td>R/W</td><td>5Ch</td><td>5C00h</td><td>00h</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>24</td></tr>
<tr><td>Description</td><td colspan="14">This command is used to set the parameters for CE2
<table>
<tr><td>Bit</td><td>Symbol</td><td>Description</td><td>Comment</td></tr>
<tr><td>D7</td><td>SLR_EN</td><td>Enable control of Sunlight Readable</td><td>0 : Disable
1 : Enable</td></tr>
<tr><td>D[6:5]</td><td>SLR_LEVEL[1:0]</td><td>Sunlight Readable Enhancement level</td><td></td></tr>
<tr><td>D4</td><td>EN_EDGE_ENH</td><td>Enable control of Edge Enhancement</td><td>0 : Disable
1 : Enable</td></tr>
<tr><td>D[3:0]</td><td>EDGE_LEVEL[3:0]</td><td>Edge enhancement Level</td><td></td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="14">-</td></tr>
<tr><td>Register Availability</td><td colspan="14">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="14">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24h</td></tr>
<tr><td>SW Reset</td><td>24h</td></tr>
<tr><td>HW Reset</td><td>24h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="14"> 
</td></tr>
</table>

RDCE2 (5D00h): Read CE2

5D00h	RDCE2											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDCE2	R	5Dh	5D00h	-	D7	D6	D5	D4	D3	D2	D1	D0	24

Description

This command is used to read the parameters for CE2

Bit	Symbol	Description	Comment
D7	SLR_EN	Enable control of Sunlight Readable	0 : Disable 1 : Enable
D[6:5]	SLR_LEVEL[1:0]	Sunlight Readable Enhancement level	
D4	EN_EDGE_ENH	Enable control of Edge Enhancement	0 : Disable 1 : Enable
D[3:0]	EDGE_LEVEL[3:0]	Edge enhancement Level	

Restriction

-

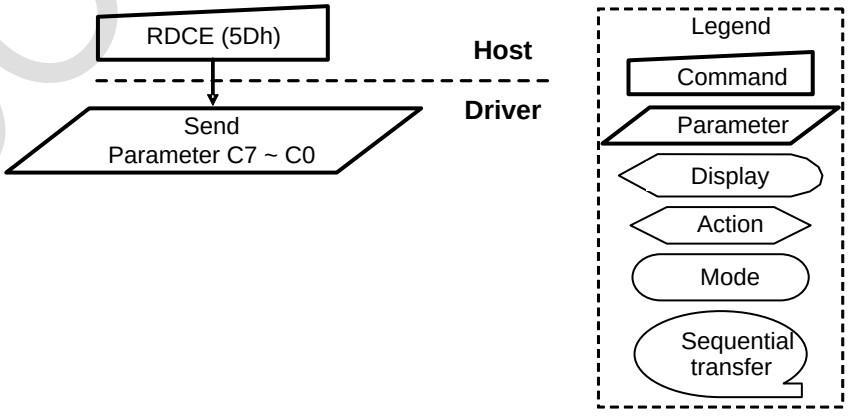
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24h
SW Reset	24h
HW Reset	24h

Flow Chart



WRCTS (6200h): Write Color Temperature Shift

6200H	WRCTS												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRCTS	R/W	62h	6200h	00h	C7	C6	C5	C4	C3	C2	C1	C0	00

Description

This command is used to set the color temperature shift away from its original state.

Bit	Symbol	Description	Comment
C7	TEMPER_EN	Color temperature shift enable	0 : Color temperature shift disable 1 : Color temperature shift enable
C6 ~ C0	TEMP_LEVEL[6:0]	Color temperature shift level	

Restriction

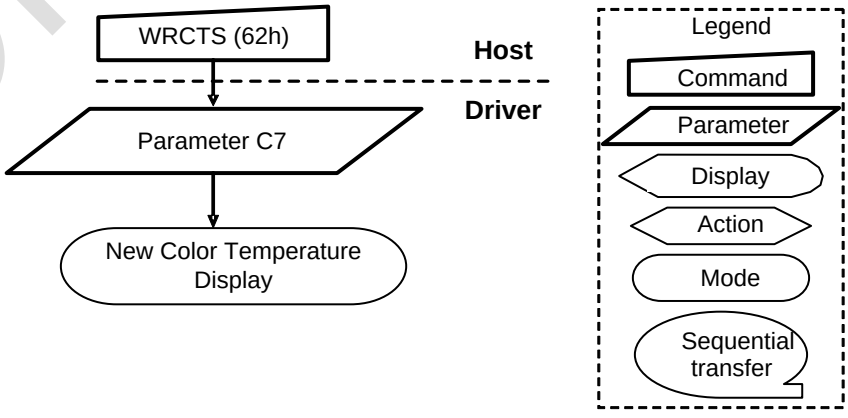
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow chart



RDCTS (6300h): Read Color Temperature Shift

6300H	RDCTS												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDCTS	R	63h	6300h	-	C7	C6	C5	C4	C3	C2	C1	C0	00

Description

This command is used to read the color temperature shift away from its original state.

Bit	Symbol	Description	Comment
C7	TEMPER_EN	Color temperature shift enable	0 : Color temperature shift disable 1 : Color temperature shift enable
C6 ~ C0	TEMP_LEVEL[6:0]	Color temperature shift level	

Restriction

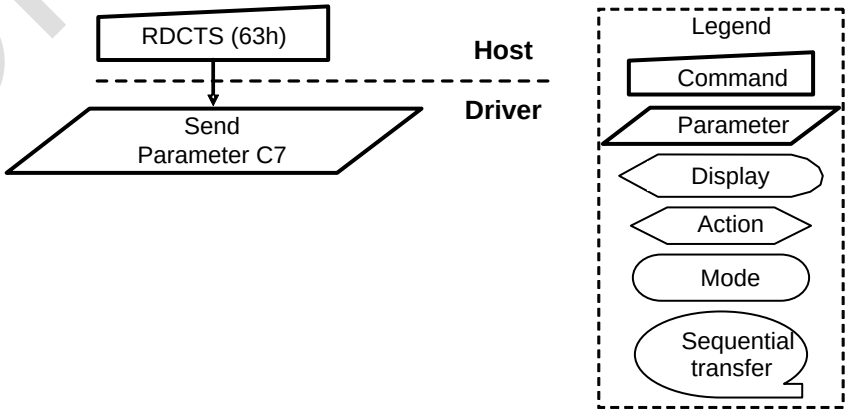
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

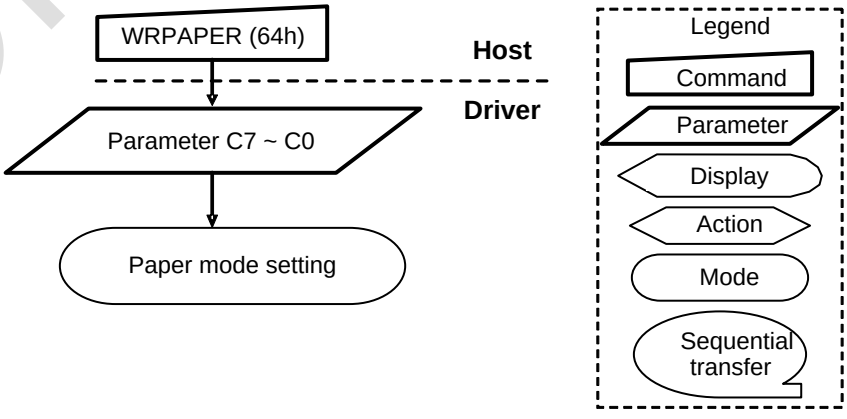
Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRPAPER (6400h): Write Paper Mode Setting

<table>
<tr><th>6400H</th><th colspan="12">WRPAPER</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Others</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>WRPAPER</td><td>R/W</td><td>64h</td><td>6400h</td><td>00h</td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set the application of paper mode.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>C7</td><td>PAPER_EN</td><td>Paper mode enable</td><td>0 : Paper mode disable
1 : Paper mode enable</td></tr>
<tr><td>C6
~
C0</td><td>PAPER_LEVEL[6:0]</td><td>Color temperature shift level for paper mode</td><td></td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">The range of color temperature shift range depends on the applied panel. .</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow chart</td><td colspan="13"> 
</td></tr>
</table>

RDPAPER (6500h): Read Paper Mode Setting

6500H	RDPAPER												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDPAPER	R	65h	6500h	-	C7	C6	C5	C4	C3	C2	C1	C0	00

Description

This command is used to read the paper mode setting.

Bit	Symbol	Description	Comment
C7	PAPER_EN	Paper mode enable	0 : Paper mode disable 1 : Paper mode enable
C6 ~ C0	PAPER_LEVEL[6:0]	Color temperature shift level for paper mode	

Restriction

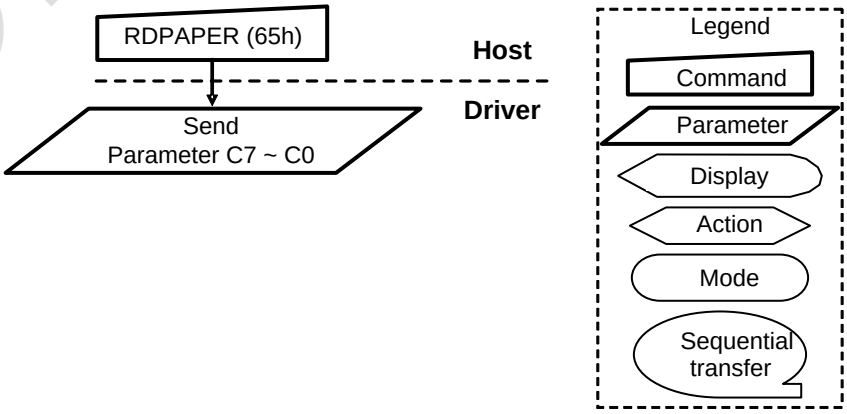
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

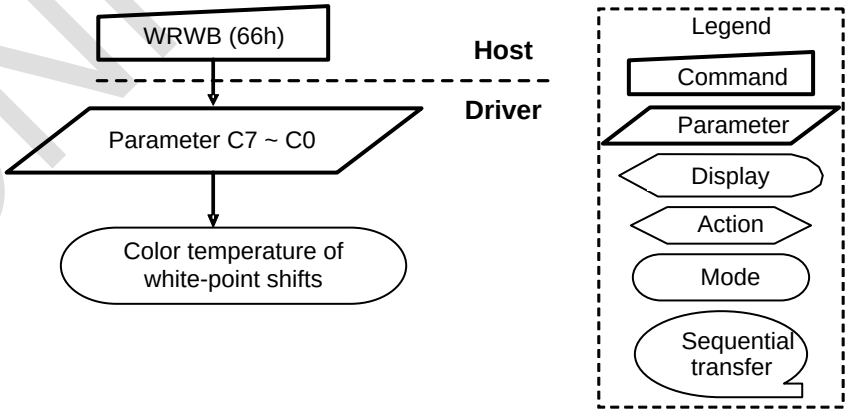
Default

Status	Default Value
Power On Sequence	00h
SW Reset	00h
HW Reset	00h

Flow Chart



WRWB (6600h): Write White Balance Control

<table>
<tr><th>6600H</th><th colspan="12">WRWB</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Others</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>WRWB</td><td>R/W</td><td>66h</td><td>6600h</td><td>00h</td><td>C7</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enable or disable white balance.
<table>
<tr><td>Bit</td><td>Symbol</td><td>Description</td><td>Comment</td></tr>
<tr><td>C7</td><td>WB_EN</td><td>White balance enable</td><td>0 : White balance disable
1 : White balance enable</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow chart</td><td colspan="13"> 
</td></tr>
</table>

RDWB (6700h): Read White Balance Control

6700H	RDWB											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDWB	R	67h	6700h	-	C7	-	-	-	-	-	-	-	00
Description	This command is used to read the paper mode setting.												

Bit	Symbol	Description	Comment
C7	WB_EN	White balance enable	0 : White balance disable 1 : White balance enable

Restriction

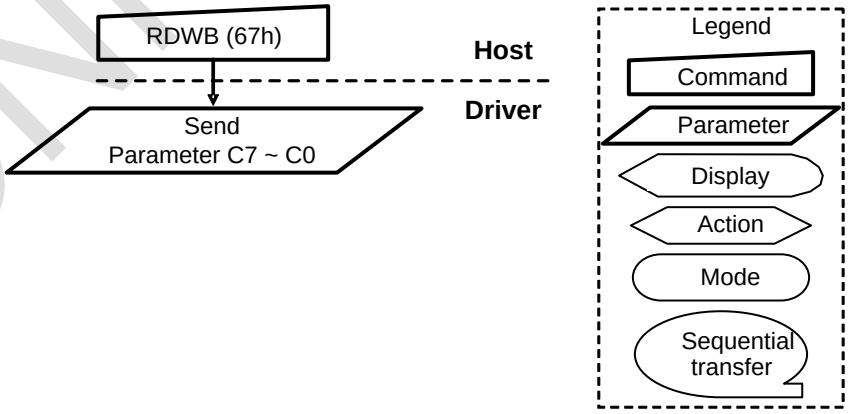
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	**00h**
SW Reset	**00h**
HW Reset	**00h**

Flow Chart



RDDDBS (A100h): Read DDB Start

A100H	RDDDBS											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDDBS	R	A1h	A100h	-	SID[7:0]								00
			A101h	-	SID[15:8]								00
			A102h	-	MID[7:0]								00
			A103h	-	MID[15:8]								00
			A104h	-	1	1	1	1	1	1	1	1	FF
Description	1st and 2nd parameter: Supplier ID code 3rd and 4th parameter: Module ID code 5th Exit code (FFh).												
Restriction													

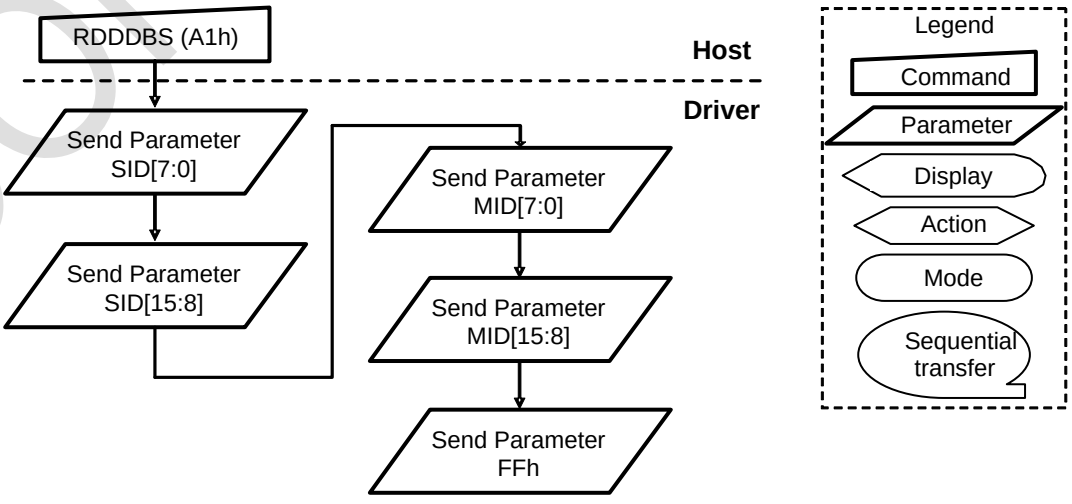
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value	
	After OTP	Before OTP
Power On Sequence	OTP Value	00h
SW Reset	OTP Value	00h
HW Reset	OTP Value	00h

Flow Chart



RDDDBC (A800h): Read DDB Continuous

A800H	RDDDBC												
Instruction	R/W	Address		Parameter									HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDDDBC	R	A8h	A800h	-	SID[7:0]								00
			A801h	-	SID[15:8]								00
			A802h	-	MID[7:0]								00
			A803h	-	MID[15:8]								00
			A804h	-	1	1	1	1	1	1	1	1	FF
Description	This command returns the supplier ID and display module mode/revision information.												
Restriction	A Read DDB-Start command (RDDDBS) should be executed at least once before a Read DDB-Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB-Continue command is undefined.												

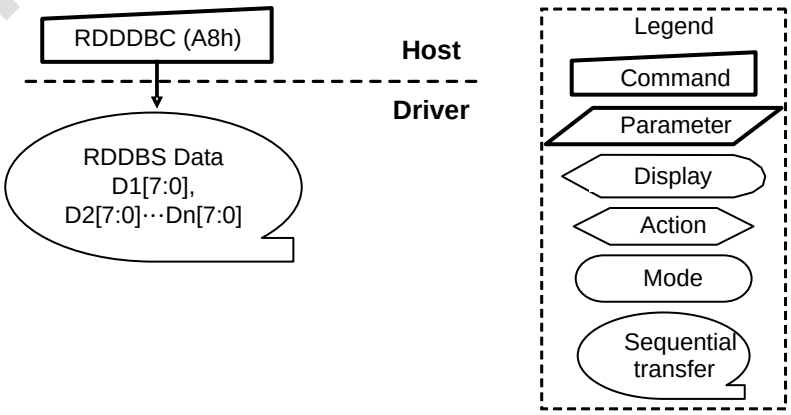
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

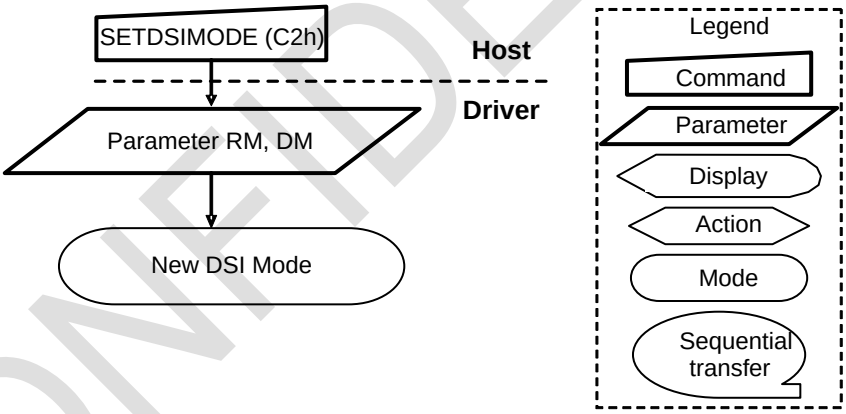
Default

Status	Default Value	
	After OTP	Before OTP
Power On Sequence	OTP Value	00h
SW Reset	OTP Value	00h
HW Reset	OTP Value	00h

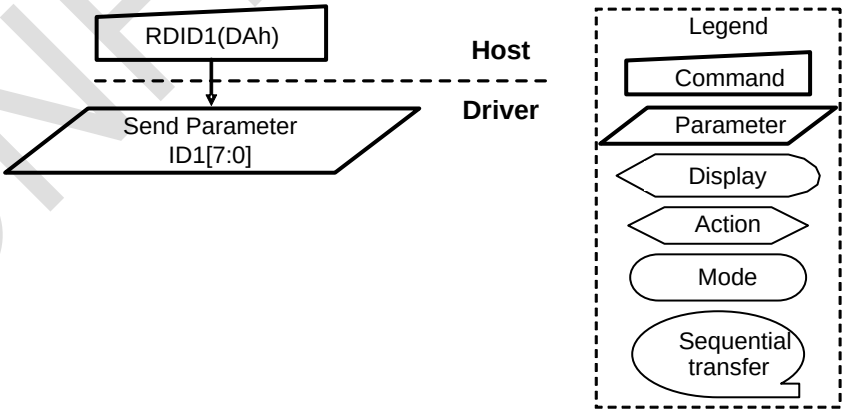
low Chart



SETDSIMODE (C200h): Set DSI Mode

<table>
<tr><th>C200H</th><th colspan="12">SETDSIMODE</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>SETDSIMODE</td><td>R/W</td><td>C2h</td><td>C200h</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>RM</td><td>0</td><td colspan="2">DM[1:0]</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to select display operation mode. When RM/DM register is changed, please follow display mode change sequence.
<table>
<tr><th rowspan="2">RM</th><th rowspan="2">DM</th><th rowspan="2">DSI mode</th><th rowspan="2">Display Data Path</th><th colspan="2">Display Timing</th></tr>
<tr><th>VSYNC</th><th>HSYNC</th></tr>
<tr><td>X</td><td>0</td><td>Command Mode</td><td>RAM -> Source</td><td>Internal</td><td>Internal</td></tr>
<tr><td>X</td><td>1</td><td>Reserved</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>X</td><td>2</td><td>Reserved</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>3</td><td>Video Mode</td><td>Bypass RAM</td><td>External</td><td>External</td></tr>
<tr><td>1</td><td>3</td><td>Video Mode</td><td>RAM -> Source</td><td>External</td><td>External</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">1. The change of DSI mode under normal display on is forbidden.
2. If the display data is of VESA compression type, W/R RAM is a must for data decompression.</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

RDID1 (DA00h): Read ID1

<table>
<tr><th>DA00H</th><th colspan="12">RDID1</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>RDID1</td><td>R</td><td>DAh</td><td>DA00h</td><td>-</td><td colspan="8">ID1[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This read byte identifies Module’s manufacture ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>After OTP</th><th>Before OTP</th></tr>
<tr><td>Power On Sequence</td><td>OTP Value</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>OTP Value</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>OTP Value</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

RDID2(DB00h) : Read ID2

DB00H	RDID2											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDID2	R	DBh	DB00h	-	ID2[7:0]								80
Description	This read byte is used to track the Module/driver version. It is changed each time a version is made to the display, material or construction specifications.												
Restriction	Parameter Range: ID2 = 0x80h to 0xFFh												

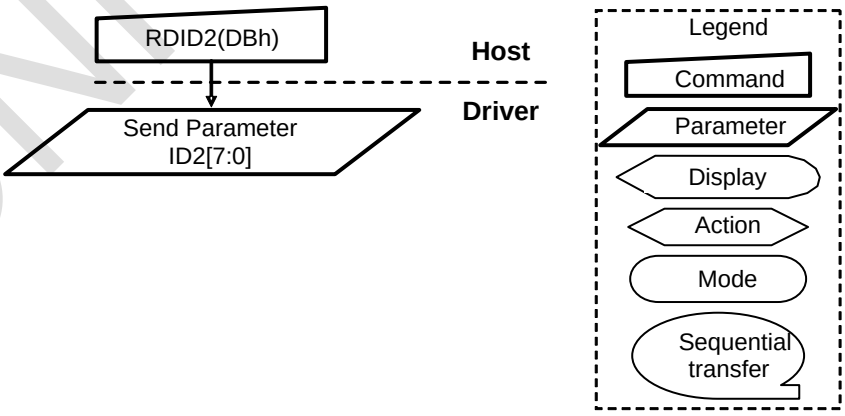
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value	
	After OTP	Before OTP
Power On Sequence	OTP Value	80h
SW Reset	OTP Value	80h
HW Reset	OTP Value	80h

Flow Chart



RDID3(DC00h) : Read ID3

DC00H	RDID3											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDID3	R	DCh	DC00h	-	ID3[7:0]								00
Description	This parameter read byte identifies Module/driver.												
Restriction													

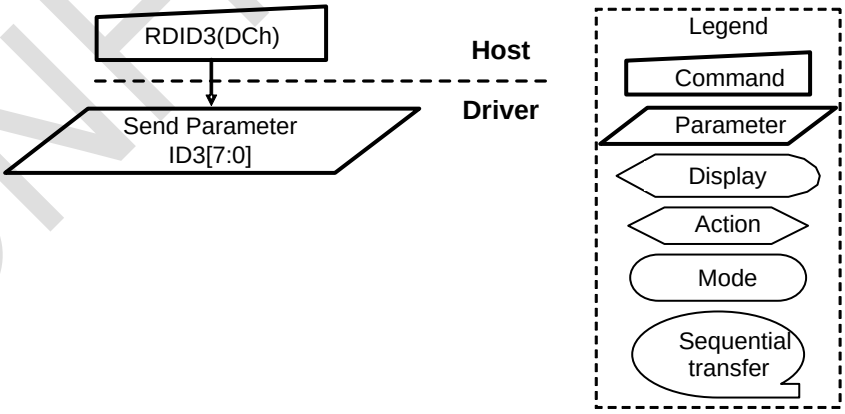
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value	
	After OTP	Before OTP
Power On Sequence	OTP Value	00h
SW Reset	OTP Value	00h
HW Reset	OTP Value	00h

Flow Chart



VESA(FA00h) : VESA function

FA00H	WRCMDPAGE											
Instruction	R/W	Address		Parameter								HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
CMDPAGESW	W/R	FAh	-	00h	0	0	0	0	0	compr_sel[1:0]		1	07h

Description

This command is VESA function control.

compr_sel[1:0]	Description
2'd0	DSC 1p1
2'd1	Reserved
2'd2	Reserved
2'd3	Raydium comprossion

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	N/A
Partial Mode On, Idle Mode On, Sleep Out	N/A
Sleep In	Yes

Default

Status	Default Value
	FAh / FA00h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

WRCMDPAGE (FE00h): Write CMD Page

<table>
<tr><th>FE00H</th><th colspan="12">WRCMDPAGE</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="8">Parameter</td><td rowspan="2">HEX</td></tr>
<tr><td>MIPI</td><td>Others</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>CMDPAGESW</td><td>W/R</td><td>FEh</td><td>-</td><td>00h</td><td colspan="8">CMD_PG_SEL[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set the command page that the driver will use.
<table>
<tr><th>CMD_PG_SEL[7:0]</th><th>Command Page</th><th>Description</th></tr>
<tr><td>8’h00</td><td>UCS</td><td>User Command Set</td></tr>
<tr><td>8’h40</td><td>MCS Page-0</td><td>General Power and Display</td></tr>
<tr><td>8’h50</td><td>MCS Page-1</td><td>Gamma Set – 1</td></tr>
<tr><td>8’h60</td><td>MCS Page-2</td><td>GOA</td></tr>
<tr><td>8’h52</td><td>MCS Page-6</td><td>Gamma Set – 2</td></tr>
<tr><td>8’h54</td><td>MCS Page-7</td><td>Gamma Set – 3</td></tr>
<tr><td>8’h20</td><td>MCS Page-10</td><td>Demura1</td></tr>
<tr><td>8’h72</td><td>MCS Page-11</td><td>BC</td></tr>
<tr><td>8’hC2</td><td>MCS page-CID</td><td>Customer ID</td></tr>
<tr><td>8hD2</td><td>MCS Page-D2</td><td>Demura2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>N/A</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>N/A</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>FEh / FE00h</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

RDCMDPAGE (FF00h): Read CMD Page

FF00H	RDCMDPAGE										
Instruction	R/W	Address		Parameter								HEX
		MIPI	Others	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDCMDPAGE	R	FFh	-	00h	CMD_PG_SEL[7:0]								00

Description

This command is used to read the command page that the driver is now in use.

CMD_PG_SEL[7:0]	Command Page	Description
8'h00	UCS	User Command Set
8'h40	MCS Page-0	General Power and Display
8'h50	MCS Page-1	Gamma Set – 1
8'h60	MCS Page-2	GOA
8'h52	MCS Page-6	Gamma Set – 2
8'h54	MCS Page-7	Gamma Set – 3
8'h20	MCS Page-10	Demura1
8'h72	MCS Page-11	BC
8'hC2	MCS page-CID	Customer ID
8hD2	MCS Page-D2	Demura2

Restriction

-

Default

Status	Default Value
	FFh / FF00h
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When device is operated beyond the absolute maximum ratings specified in this table, it may be permanently damaged. It is strongly recommended to use this device within the specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this driver IC will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage – (I)	VCC, VDDI, VDDAM	6.6	V
Power Supply Voltage –(II)	VDDA, VDDB, VDDR	6.6	V
Power Supply Voltage –(III)	AVDD-AVSS	8.8	V
	AVEE-AVSS	-6.6	V
Supply voltage (HV)	VGH – VGL	33	V
MIPI Differential Input	HSSI_CLK_P/N_A / HSSI_CLK_P/N_B HSSI_D0_P/N_A / HSSI_D0_P/N_B HSSI_D1_P/N_A / HSSI_D1_P/N_B HSSI_D2_P/N_A / HSSI_D2_P/N_B HSSI_D3_P/N_A / HSSI_D3_P/N_B	1.5	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI + 0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI + 0.3	V
Operating temperature	Topr	-40 ~ 85	°C
Storage temperature	Tstg	-55 ~ 125	°C

7.2 ESD Protection Level

Model	Test Condition	Level
Human Body Mode	R = 1.5 kohm / C = 100 pF	≥ 2KV
Machine Mode	R = 0 ohm / C = 200 pF	≥ 200V

7.3 Latch-Up Protection Level

The device will not latch up at trigger current levels less than ±200mA.

7.4 Max Series Resistance

The driver will operate in “Chip on Glass” applications with series resistances (due to ITO track resistance). Voltages are specified at module I/O assuming maximum values as in below table.

Name	Type	Maximum Series Resistance	Unit
VDDI	Power supply	5	Ω
VDDA, VDDB, VDDR	Power supply	3	Ω
VCC, VDDAM	Power supply	3	Ω
DVDD, MVDDA1, MVDDA2	Power supply	3	Ω
AVDD	Power supply	3	Ω
VSSI	Power supply	5	Ω
DVSS	Power supply	3	Ω
VSSA,VSSB, VSSR, AVSS	Power supply	3	Ω
VSSAM	Power supply	3	Ω
PSWAP_A, PSWAP_B DSWAP_A[1:0], DSWAP_B[1:0] PNSLV DB_MODE[2:0] IM[1:0], BSTM IM_PORT_AB	Input	100	Ω
RESX	Input	50	Ω
SDI_RDX, WRX_SCL	I2C	30	Ω
AVDD_EN, SWIRE TE, TE1 PCD, ERR_FG	Output	20	Ω
TEST[1]_F_CSB, TEST[2]_F_SCLK TEST[3]_F_SDI, TEST[4]_F_SDO TEST[5]_F_HOLDN TEST[6]_F_WPN TEST[7]_F_DISS	Flash Pin	10	Ω
HSSI_CLK_P/N_A, HSSI_CLK_P/N_B HSSI_D0_P/N_A, HSSI_D0_P/N_B HSSI_D1_P/N_A, HSSI_D1_P/N_B HSSI_D2_P/N_A, HSSI_D2_P/N_B HSSI_D3_P/N_A, HSSI_D3_P/N_B	Input	5	Ω
VGMP, VGSP	Regulator Output	5	Ω
VREP/VREFN/VREF	Regulator Output	5	Ω
VGH/VGL VGHR/VGLR	Charge Pump Regulator Output	5	Ω
OVDD_INT/OVSS_INT	Regulator Output	2	Ω
C21P/N, C22P/N C31P/N, C32P/N C41P/N, C42P/N C51P/N, C52P/N	Capacitor Connection	5	Ω
AVEE, VCL	Charge Pump	5	Ω
MTP_PWR	Power supply	5	Ω

Note : The impedance matching among MIPI interface I/O is very critical for high-speed data receving.

7.5 DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply	VCI		2.7	3.0	3.6	V
AVDD Input Level	AVDD		4.5		8.0	V
Digital I/O Power Supply (non-MIPI I/O)	VDDI	Digital I/O supply voltage	1.62	1.8	1.98	V
Digital I/O Input Level @Logic High	VIH	VDDI = 1.62V ~ 1.98	0.7* VDDI	-	VDDI	V
Digital I/O Input Level @Logic Low	VIL	VDDI = 1.62V ~ 1.98V	0.0	-	0.3* VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1 mA	0.8* VDDI	-	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1 mA	0.0	-	0.2* VDDI	V
Digital I/O Input leakage @ Logic High	IIHD	Vin = VDDI			1	uA
Digital I/O Input Leakage @Logic Low	IILD	Vin = 0	-1			uA
MIPI I/O Power Supply	MVDDL	MIPI I/O supply voltage	-	1.2	-	V
MIPI Input leakage @Logic High	IIHD	Vin = MVDDL			1	uA
MIPI Input leakage @Logic Low	IILD	Vin = 0	-1			uA
AVEE booster voltage	AVEE	AVEE = -1*AVDD	-6.5		-4.5	V
VCL booster voltage	VCL	VCL = -1*VCI	-	-2.5	-	V
VGH booster voltage	VGH				2*AVDD - AVEE	V
VGL booster voltage	VGL		2*AVEE - AVDD			V
Maximum voltage between VGH and VGL	VGHL	|VGH-VGL|			30	V
Panel Reference Voltage	VREFP	VREFP=VREFPO	0.2		AVDD-0.3	V
	VREFN	VREFN=VREFNO	AVEE+0.3		-0.2	V
GOA Output Voltage	VGHR	VGHR=VGLO	3		VGH-0.5V	V
	VGLR	VGLR=VGLO	VGL+0.5V		-3	V
Gamma Reference Voltage	VGMP		2.0		AVDD-0.3	V
	VGSP		0.3		5.0	V
Source Output Offset (chip to chip)	V_{OFFSET}			TBD		mV
Source Output Deviation (channel to channel)	$V_{DEV,POS}$	Sout ≥ AVDD-1.0V, and 0V < Sout ≤ 1.0V		TBD		mV
		1.0V < Sout < AVDD-1.0V		TBD		mV
OTP Power Supply	MTP_PWR	OTP Programming Supply Voltage	5.75	6	6.25	V

7.6 DSI Timing Characteristics

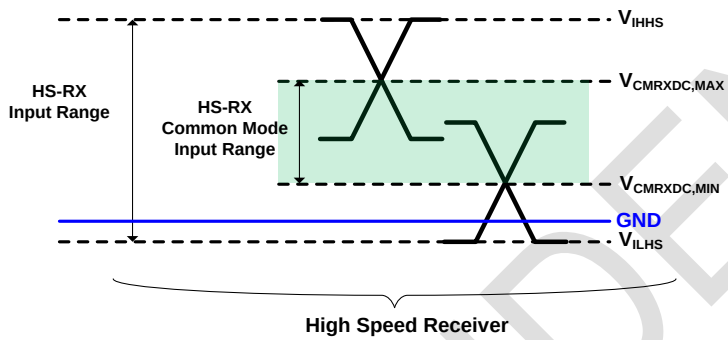
7.6.1 Receiver Characteristics

■ High-Speed Receiver

The differential input high and low threshold voltages of the HS receiver are denoted by V_{IDTH} and V_{IDTL}, respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively. V_{CMRXDC} is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its DP and DN input signal pins when both signal voltages, V_{DP} and V_{DN}, are within the common-mode voltage range and if the voltage difference of V_{DP} and V_{DN} exceeds either V_{IDTH} or V_{IDTL}. The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode interference $\Delta V_{CMRX(HF)}$ and $\Delta V_{CMRX(LF)}$.

During operation of the HS receiver, termination impedance Z_{ID} is required between the DP and DN pins of the HS receiver. Z_{ID} shall be disabled when the module is not in the HS receive mode.

C_{CM} is the common-mode AC termination, which ensures a proper termination of the receiver at higher frequencies. For higher data rates, C_{CM} is needed at the termination centre tap in order to meet the common-mode reflection requirements.



HS Receiver Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_{CMRXDC}	Common-mode voltage for HS receiver	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
Z_{ID}	Differential input impedance	80	100	125	Ω	
C_{CM}	Common-mode termination			60	pF	3

Notes:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. Values in this table include a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz
3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.
4. Voltage difference compared to the DC average common-mode potential.

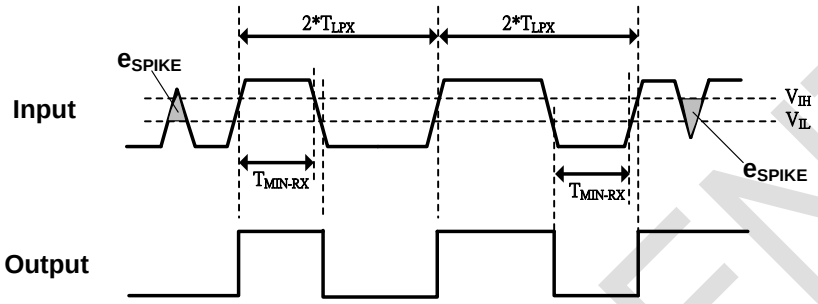
■ Low-Power Receiver

The Low-Power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin.

The input low-level voltage, V_{IL}, is the voltage at which the receiver is required to detect a low state in the input signal. A lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the Ultra-Low Power State. V_{IL} is larger than the maximum single-ended Line voltage during HS transmission. Therefore, a LP receiver shall detect low during HS signaling.

The input high-level voltage, V_{IH}, is the voltage at which the receiver is required to detect a high state in the input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a hysteresis, defined as V_{HYST}.

The LP receiver shall reject any input signal smaller than e_{SPIKE}. Signal pulses wider than T_{MIN-RX} shall propagate through the LP receiver.



Low-Power Receiver Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	
eSPIKE	Input pulse rejection			300	V*ps	1
TMIN-RX	Minimum pulse width response	20			ns	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. An impulse less than this will not change the receiver state. An input pulse greater than this shall toggle the output.

7.6.2 Transmitter Characteristics

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low.

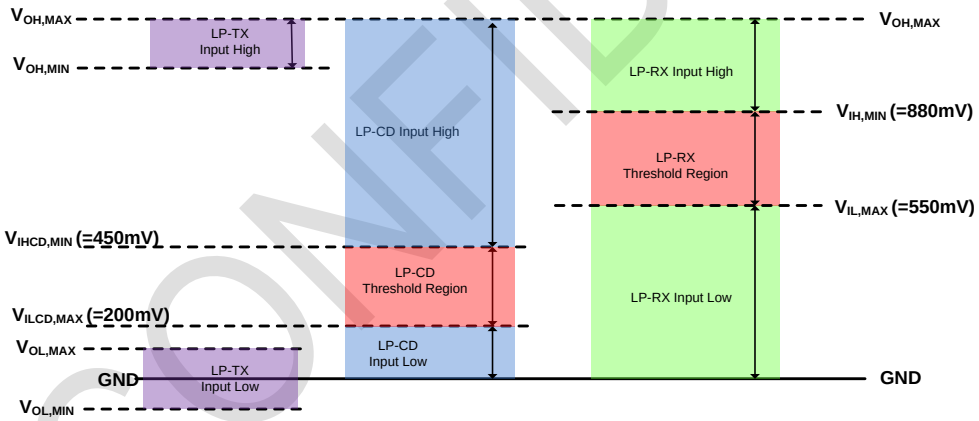
Low-Power Transceiver Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	

Notes:
(1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state an impulse less than this will not change the receiver state.
(2) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers. Input Glitch Rejection of Low Power Receivers as follow.

■ Line Contention Detection

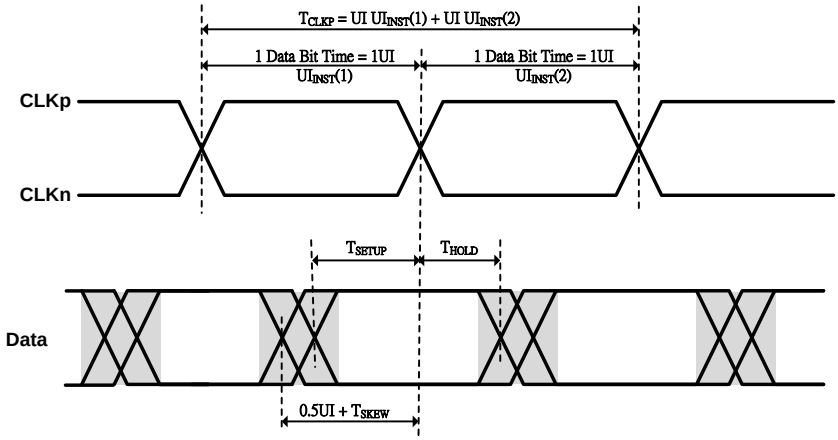
The Low-Power receiver and a separate Contention Detector (LP-CD) shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-Power signal. This is required to detect line contention. The LP-CD shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD}. An LP low fault shall not be detected when the pin voltage is less than V_{ILCD}. The LP-CD threshold voltages are shown along with the normal signaling voltages in the following figure.



Contention Detector (LP-CD) DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
V_{IHCD}	Logic 1 contention threshold	450			mV	
V_{ILCD}	Logic 0 contention threshold			200	mV	

■ Data to Clock Timing Definitions



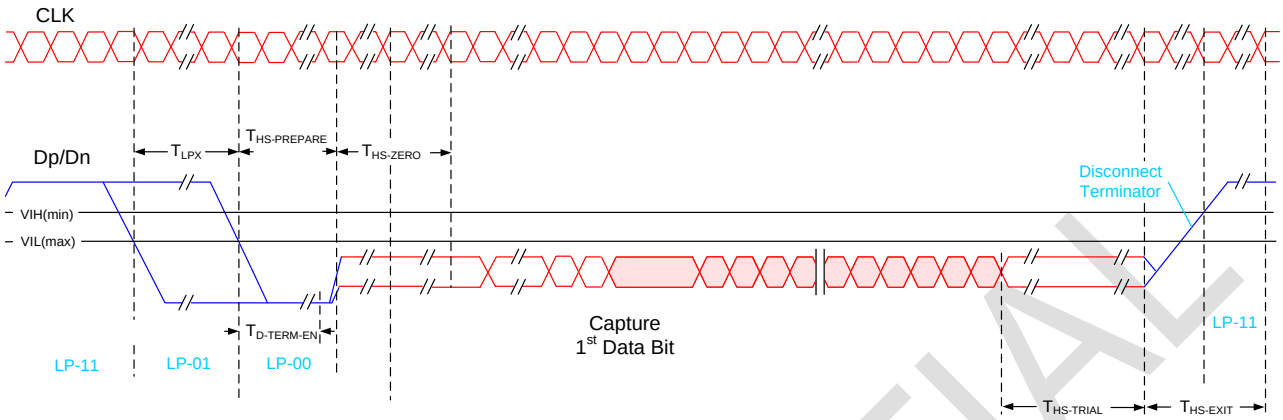
■ Data-Clock Timing Specifications:

Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	1		12.5	ns	1,2
Data-to-Clock Skew	T_{SKEW}	-0.15		0.15	UI_{INST}	3
Data-to-Clock Setup Time (Receiver side)	T_{SETUP}	0.15			UI_{INST}	4
Clock-to-Data Hold Time (Receiver side)]	T_{HOLD}	0.15			UI_{INST}	4

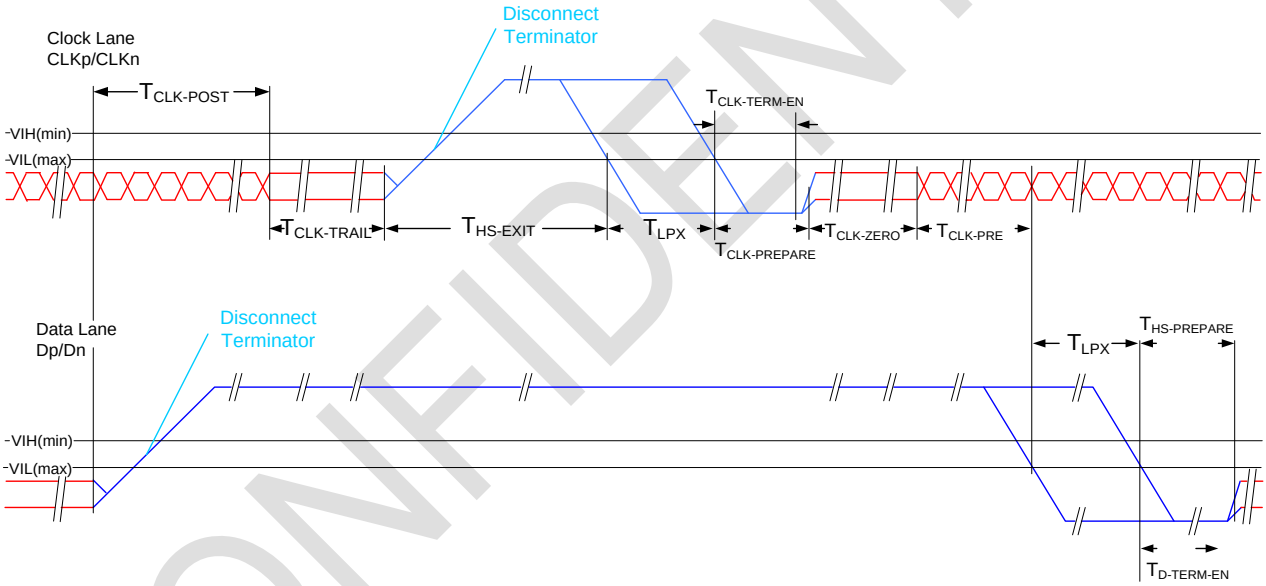
Notes:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
3. Total silicon and package delay budget of 0.3*UI_{INST}
4. Total setup and hold window for receiver of 0.3*UIINST

7.6.3 DSI Timing Specification

■ HS Data Transmission Burst



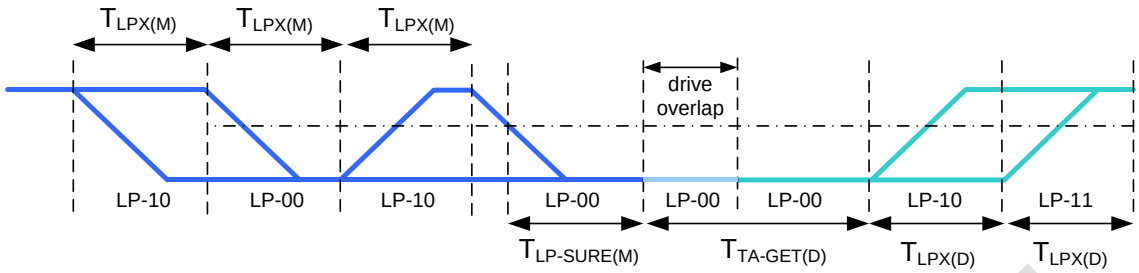
■ HS clock transmission



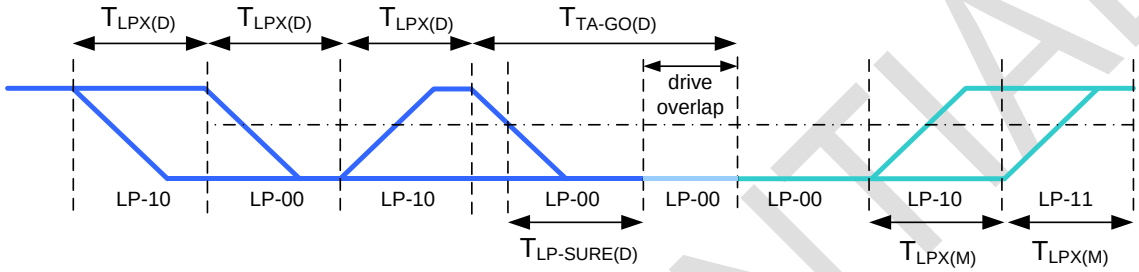
■ Timing Specifications for HS Transmission:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	-		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	-		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
$T_{AB-SKEW}$	Timing Skew between Port A and Port B			100	ns

■ Bus Turnaround Procedure (From MPU to display module)



Bus turnaround (BAT) timing



Bus turnaround (BAT) from display module to MPU timing

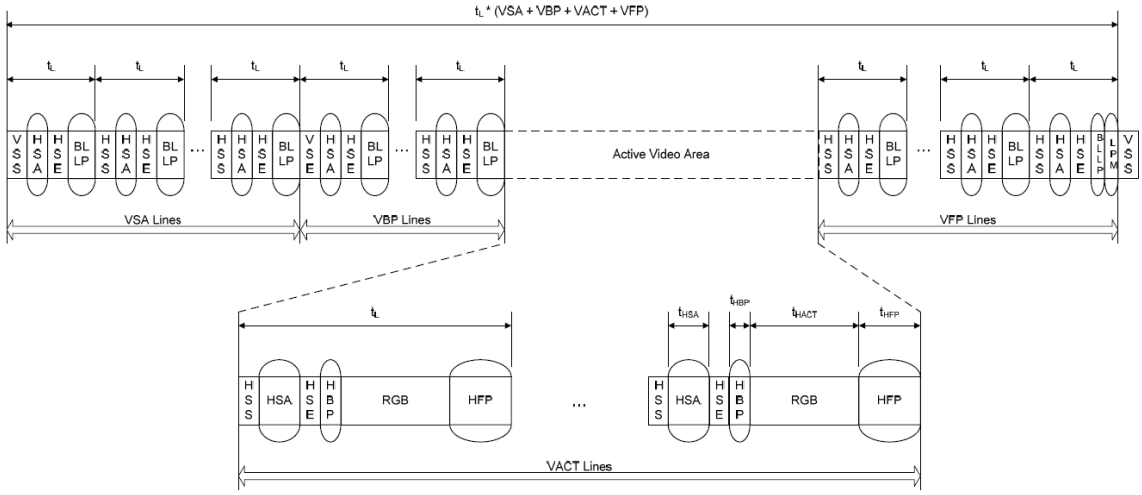
■ Timing Specifications for Low Power Transmission:

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

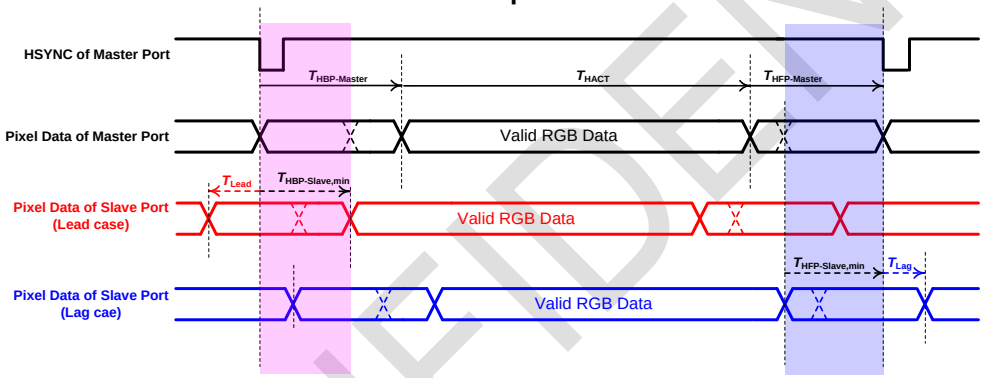
Notes:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

7.6.4 Video Mode Interface Timing Specification

■ **DSI Video Mode Interface Timing**



■ **Data Transmission of Dual MIPI-DSI ports**



■ **Timing specification of Video Mode Data Transmission**

Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes		250	-	1000	Mbps
T_{LINE}	Line time	WQXGA/WQHD	-	6.47, note1	-	us
T_{HBP}	Horizontal back porch	-	0.5	-	-	us
T_{HACT}	Time for image data	WQXGA (8 data lanes)	4.8, note3	-	19.2	us
T_{HACT}	Active pixel per line	WQXGA	-	1600	-	pixels
T_{HFP}	Horizontal front porch	-	0.5	-	-	us
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	-	8, note2	-	H
VACT	Active lines per frame	-	-	2560	-	H
VFP	Vertical front porch	-	note4	8, note2	-	H

Notes
1. Frame rate (Typ)=60Hz, VBP=8, and VFP=8.
2. VBP and VFP value depends on GOA timing.
3. For WQXGA(1600 pixels), tHACT=24*1600/8GHz=4.8us
4. For IIX demura, the VFP must be ≥ Dummy DE Line. Hence that for resolution 2992, VFP must be ≥ 16H.
5. The restriction of Thbp+Thfp ≥1us is for each line return LP. If no return LP, the Thbp(min)= 0.1us and Thfp(min)=0.15us

HD (720x1280) Video Mode Timing Table

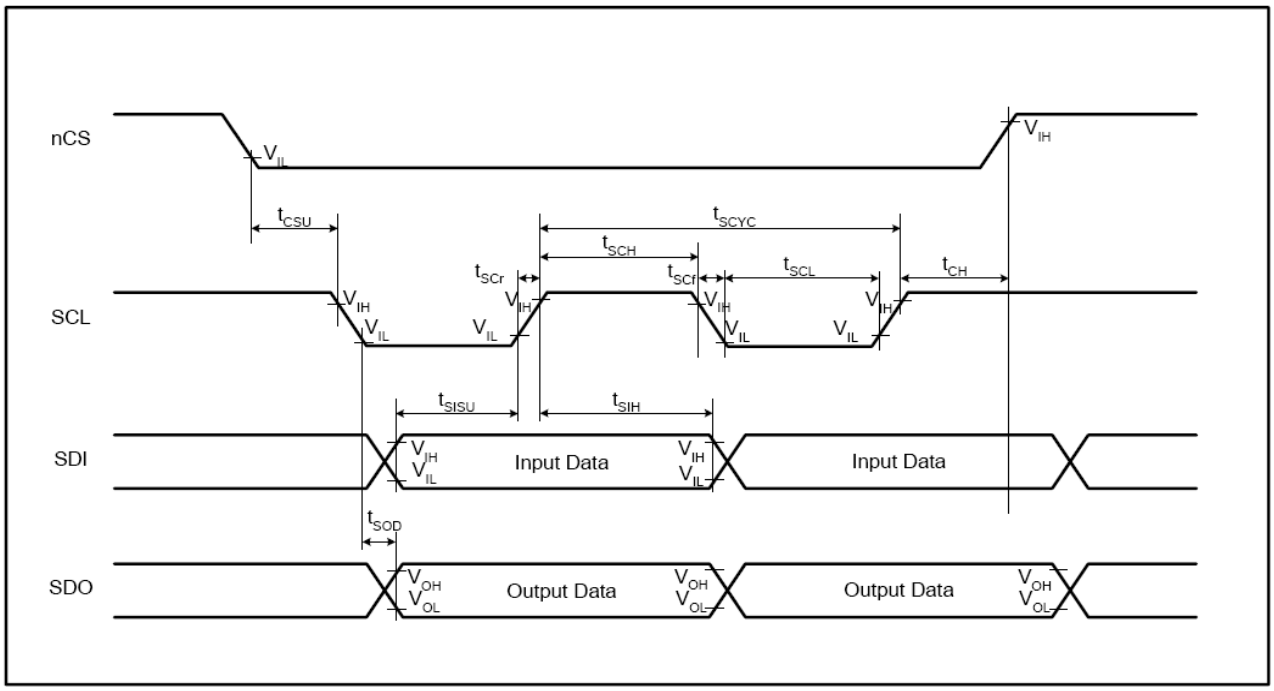
Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes		250	-	1000	Mbps
T_{LINE}	Line time	HD	-	12.86, note1	-	us
T_{HBP}	Horizontal back porch	-	0.5, note4	-	-	us
T_{HACT}	Time for image data	HD (2 data lanes) HD (3 data lanes) HD (4 data lanes)	8.64, note3 5.76 4.32	-	-	us
T_{HACT}	Active pixel per line	WQXGA	-	720	-	pixels
T_{HFP}	Horizontal front porch	-	0.5, note4	-	-	us
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	-	8, note2	-	H
VACT	Active lines per frame	-	-	1280	-	H
VFP	Vertical front porch	-	-	8, note2	-	H

Notes
1. Frame rate (Typ)=60Hz, VBP=8, and VFP=8. T_{LINE}= 1/60/(1280+8+8)= 12.86us
2. VBP and VFP value depends on GOA timing.
3. For HD, T_{HACT}=24*720/2GHz=8.64us for 2 data lanes
4. Each line return LP, min. HBP= 0.5us, HFP= 0.5us
5. The restriction of Thbp+Thfp ≥1us is for each line return LP. If no return LP, the Thbp(min)= 0.1us and Thfp(min)=0.15us

FHD (1080x1920) Video Mode Timing Table

Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes		250	-	1000	Mbps
T_{LINE}	Line time	FHD	-	8.609	-	us
T_{HBP}	Horizontal back porch	-	0.5	-	-	us
T_{HACT}	Time for image data	FHD (4 data lanes)	6.48	-	-	us
T_{HACT}	Active pixel per line	-	-	1080	-	pixels
T_{HFP}	Horizontal front porch	-	0.5	-	-	us
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	-	8	-	H
VACT	Active lines per frame	-	-	1920	-	H
VFP	Vertical front porch	-	-	8	-	H

7.7 SPI Timing Characteristics



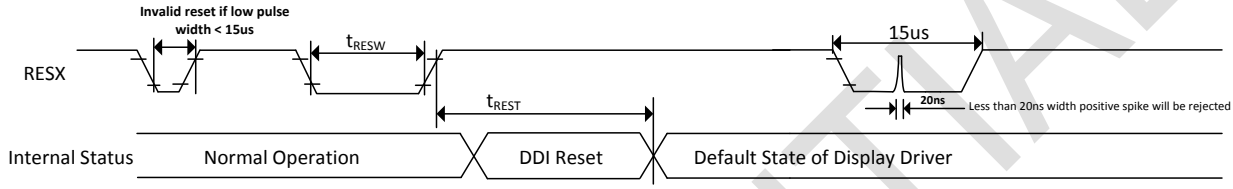
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		ns	-
	T_{SCYC}	Clock cycle (Read)	300		ns	
	T_{SCH}	Clock “H” pulse width (Write)	40		ns	
	T_{SCH}	Clock “H” pulse width (Read)	140		ns	
	T_{SCL}	Clock “L” pulse width (Write)	40		ns	
	T_{SCL}	Clock “L” pulse width (Read)	140		ns	
	T_{SCr}	Clock rise time		5	ns	
	T_{SCf}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	20		ns	-
	T_{CH}	Chip select hold time	50		ns	
SDI	T_{SISU}	Data input setup time	20		ns	-
	T_{SIH}	Data input hold time	20		ns	
SDO	T_{SOD}	Data output setup time		120	ns	-
	T_{SOH}	Data output hold time	5		ns	

Notes:
(1) Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.
(2) Ta = -40°C to 85°C, VDDI=1.62V to 1.98V, VCI=2.5V to 3.6V, GND=0V

7.8 Reset Timing Characteristics

If Reset starts in Sleep-Out mode the display driver will enter blanking sequence with maximum time 120 msec. On the other hand, the display driver will remain in blanking state if Reset occurs in Sleep-In mode and then return to IC's default sate soon after H/W reset. "Spike Rejection" also applies during a valid reset pulse as shown below.

During reset complete time (t_{REST}), data in MTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 10ms after the rising edge of RESX. Therefore, it is necessary to wait at least 10ms after releasing RESX before sending commands. Also, the rising edge of RESX to Sleep-Out command should be longer than120msec.



Reset timing @VDDI=1.62V to 1.98V, VSSA=DVSS=VSSI=0V, Ta=-40℃ to 85℃

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	Reset low pulse width	15	-	-	1. Shorter than 5us, Reset rejected 2. Longer than 15μs, IC reset 3. Between 5μs and 15μs, It depends on voltage and temperature condition.	μs
t_{REST}	Reset complete time	-	-	10	When reset applied at sleep-in mode	ms
		-	-	120	When reset applied at sleep-out mode	ms

8. Power Structure and On/Off Sequence

8.1 Power Mode Summary

■ **BSTM Control**

BSTM	Power Mode	Note
0	Reserved	Reserved
1	2-power mode (VDDI + VCI) + Power IC	External component: Power IC + flying capacitors

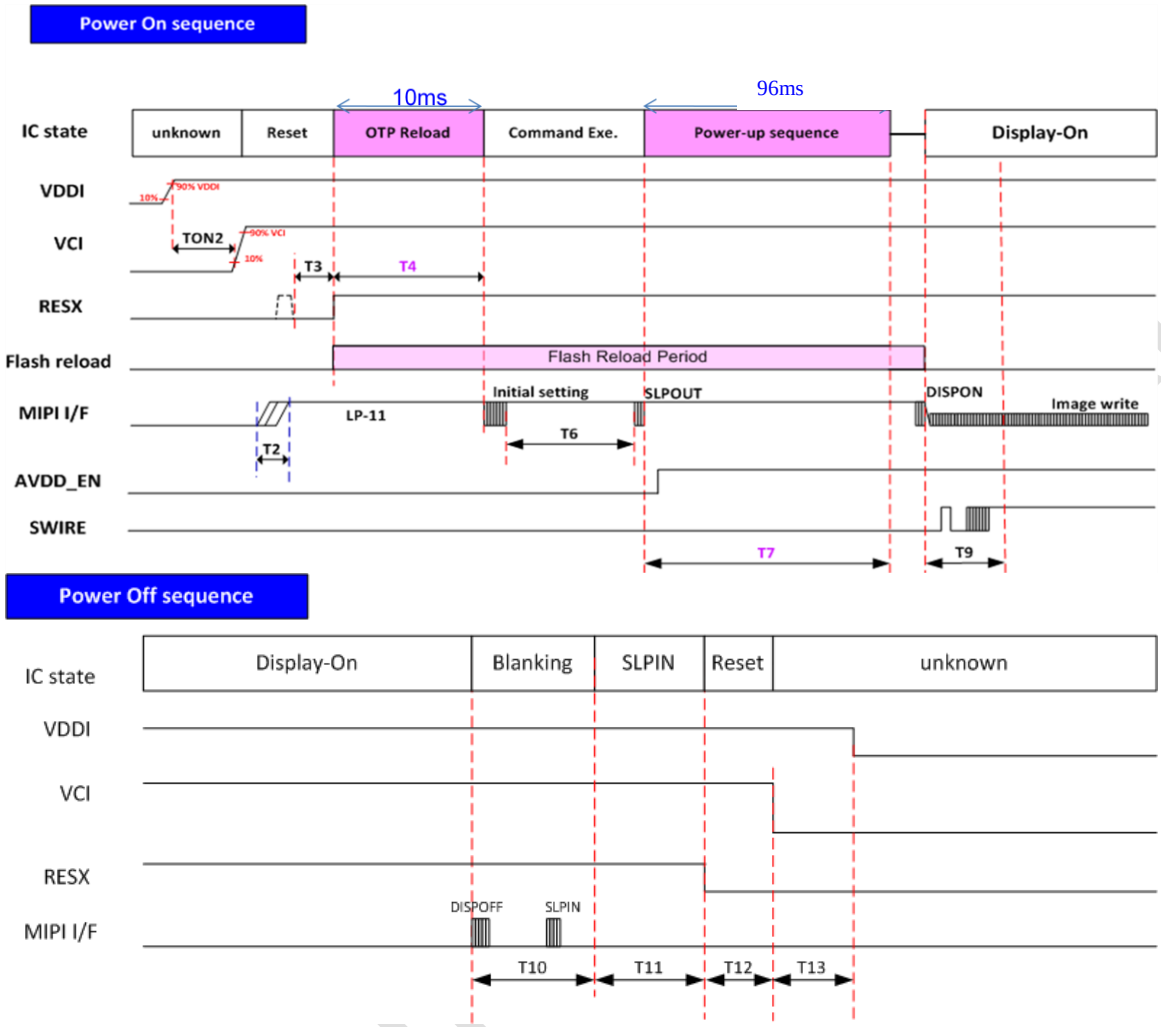
■ **Timing Specification of Power On/Off Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
TON2	2	-	-	ms	
T2	1	-	-	ms	MIPI stabilization time
T3	1	-	-	ms	Effective hardware reset period
T4	10	-	-	ms	OTP reload time
T6	0	-	-	ms	Initial code input finish to SLPOUT command input
T7	-	96	-	ms	Normal power-up sequence
T9	2	-	-	VS	Display-On Blanking region
T10	2	-	-	VS	Display-Off blanking region
T11	1	-	-	VS	Blanking region
T12	1	-	-	ms	Effective hardware reset period
T13	2	-	-	ms	Power off period

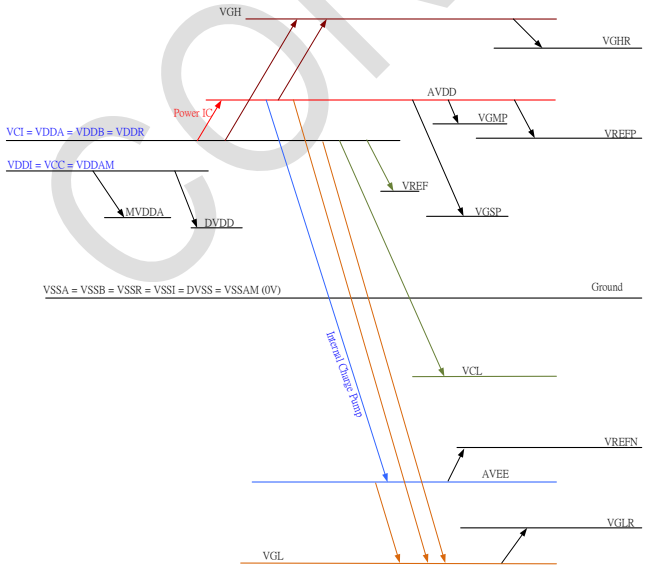
Notes:
(1) VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

8.2 Power Generation for 2-Power Mode

■ Power Sequence and Generation

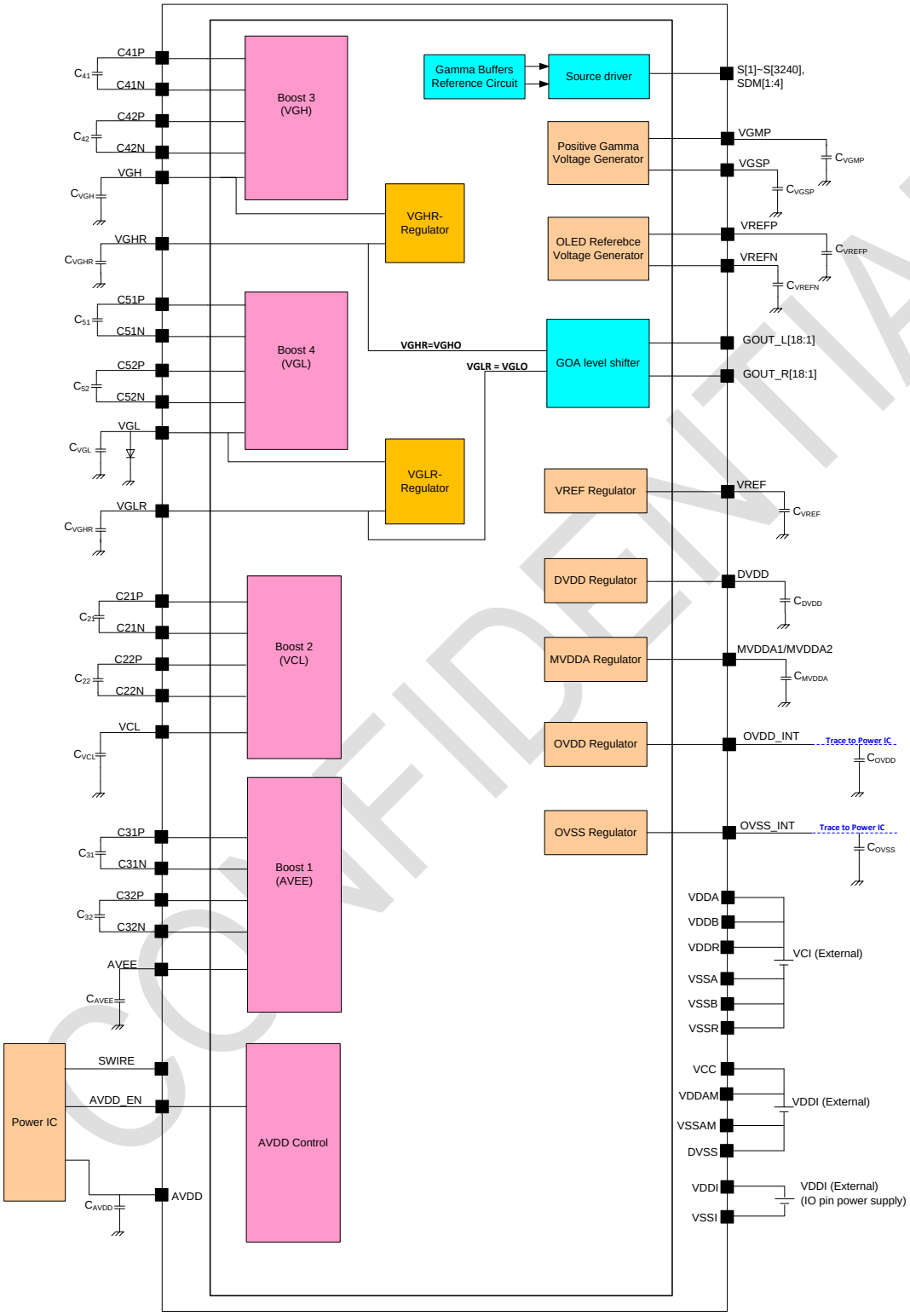


■ Architecture of Internal Power Generation



8.3 Application Circuit for 2-Power Mode

■ Application Circuit

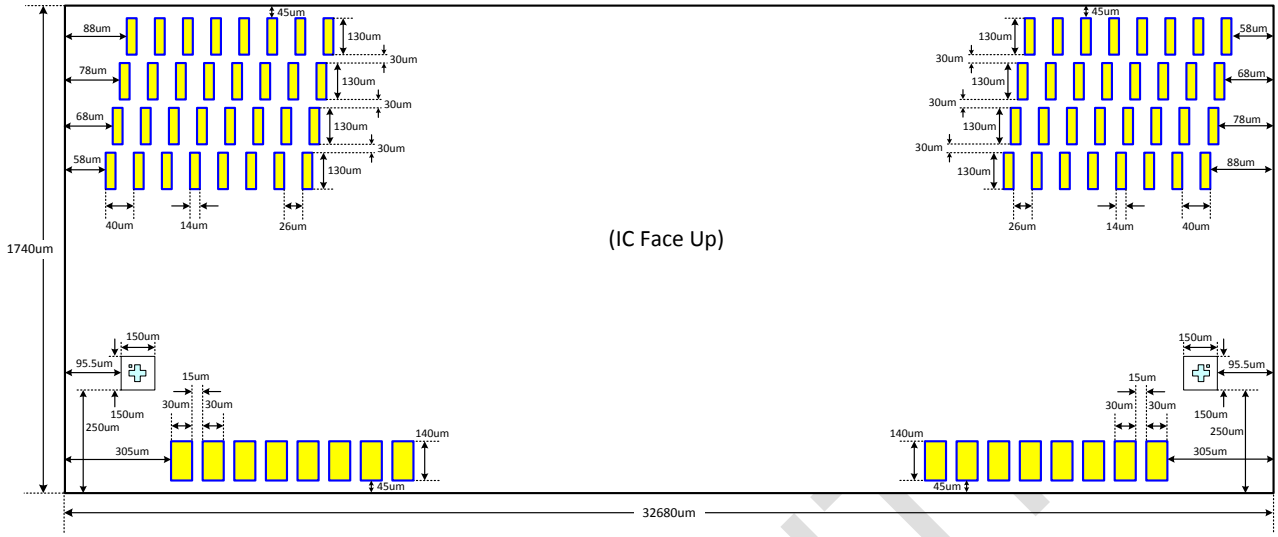


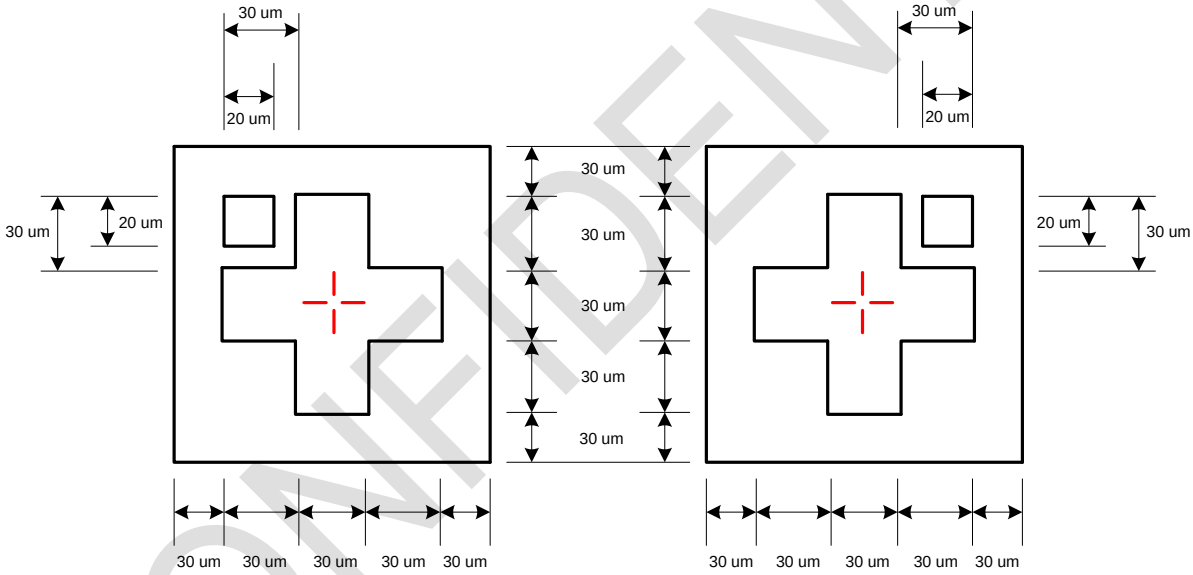
■ **Recommended External Component**

No.	Signal name	Values	Max ability	Note
1	VDDA, VDDR, VDDB	Cap , 2.2uF	6.3V	
2	VDDI, VCC, VDDAM	Cap , 2.2uF	6.3V	
3	AVDD	Cap , 2.2uF	10V	
4	DVDD	Cap , 4.7uF	6.3V	
5	MVDDA	Cap , 4.7uF	6.3V	
6	VREF	Cap , 22nF	6.3V	
7	VREFN	Cap , 2.2uF	10V	
8	VREFP	Cap , 2.2uF	10V	
9	VGMP	Cap , 1.0uF	10V	
10	VGSP	Cap , 1.0uF	10V	
11	C21P-C21N	Cap , 1.0uF	6.3V	VCL-pump
12	C22P-C22N	Cap , 1.0uF	6.3V	
13	VCL	Cap , 2.2uF	6.3V	
14	C31P-C31N	Cap , 1.0uF	10V	AVEE-pump
15	C32P-C32N	Cap , 1.0uF	10V	
16	AVEE	Cap , 2.2uF	10V	
17	C41P-C41N	Cap , 1.0uF	16V	VGH-pump
18	C42P-C42N	Cap , 1.0uF	16V	
19	VGH	Cap , 2.2uF	25V	
20	VGHR	Cap , 1.0uF	25V	
21	C51P-C51N	Cap , 1.0uF	16V	VGL-pump
22	C52P-C52N	Cap , 1.0uF	16V	
23	VGL	Cap , 2.2uF	25V	
24	VGLR	Cap , 1.0uF	25V	
25	VGL-GND	Schottky Diode		
26	OVDD_INT	Cap , 4.7uF	10V	On FPC for AOD
27	OVSS_INT	Cap , 4.7uF	10V	On FPC for AOD

Notes:
1. There are totally 26 capacitors and 1 diode are necessary at most.
2. For most applications, either VREFP or VREFN is needed. So, the capacitor for the unused one can be saved.
3. The Schottky diode of VGL-GND is a must which is to prevent from power-on latch-up occurrence.

9. Pad Diagram for COG





- **Chip Size= 32680um x 1740um (includes scribe line and seal ring)**
- **Chip Thickness= 200um**
- **Au Bump:**
  1. **ILB Size= 30um x 140um, Pitch= 45um**
  2. **OLB Size= 14um x 130um, Pitch= 40um**
  3. **Bump Height= 12±2um (Typ.)**
- **Alignment Mark L coordinate: (-16169.5um, -545um)**
- **Alignment Mark R coordinate: (16169.5um, -545um)**

◆ Source Output for Different Resolution

H-Resolution	SPR / Real	Channel No	Active Source Output
1600	2/3 SPR	3200	S[1] ~ S[1600], S[1641] ~ S[3240]
1440	2/3 SPR	2880	S[1] ~ S[1440], S[1801] ~ S[3240]
1440	SPR Bypass	2880	S[1] ~ S[1440], S[1801] ~ S[3240]
1080	Real	3240	S[1] ~ S[3240]
1080	2/3 SPR	2160	S[1] ~ S[1080], S[2161] ~ S[3240]