42.0 inch E-paper Display Series

GDEP420T01

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**42.0" E-PAPER DISPLAY**
Model Name	**GDEP420T01**
Date	**2023/01/06**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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1. Overview

GDEP420T01 is a reflective electrophoretic technology display module based on active matrix TFT substrate. It has 42" active area with 2160 x 2880 pixels and 3:4 aspect ratio. The display is capable to display images at 2 to 16 gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

2.Features

High contrast electrophoretic imaging film

2160 x 2880 display

Ultra low power consumption

Pure reflective mode

Bi-stable display

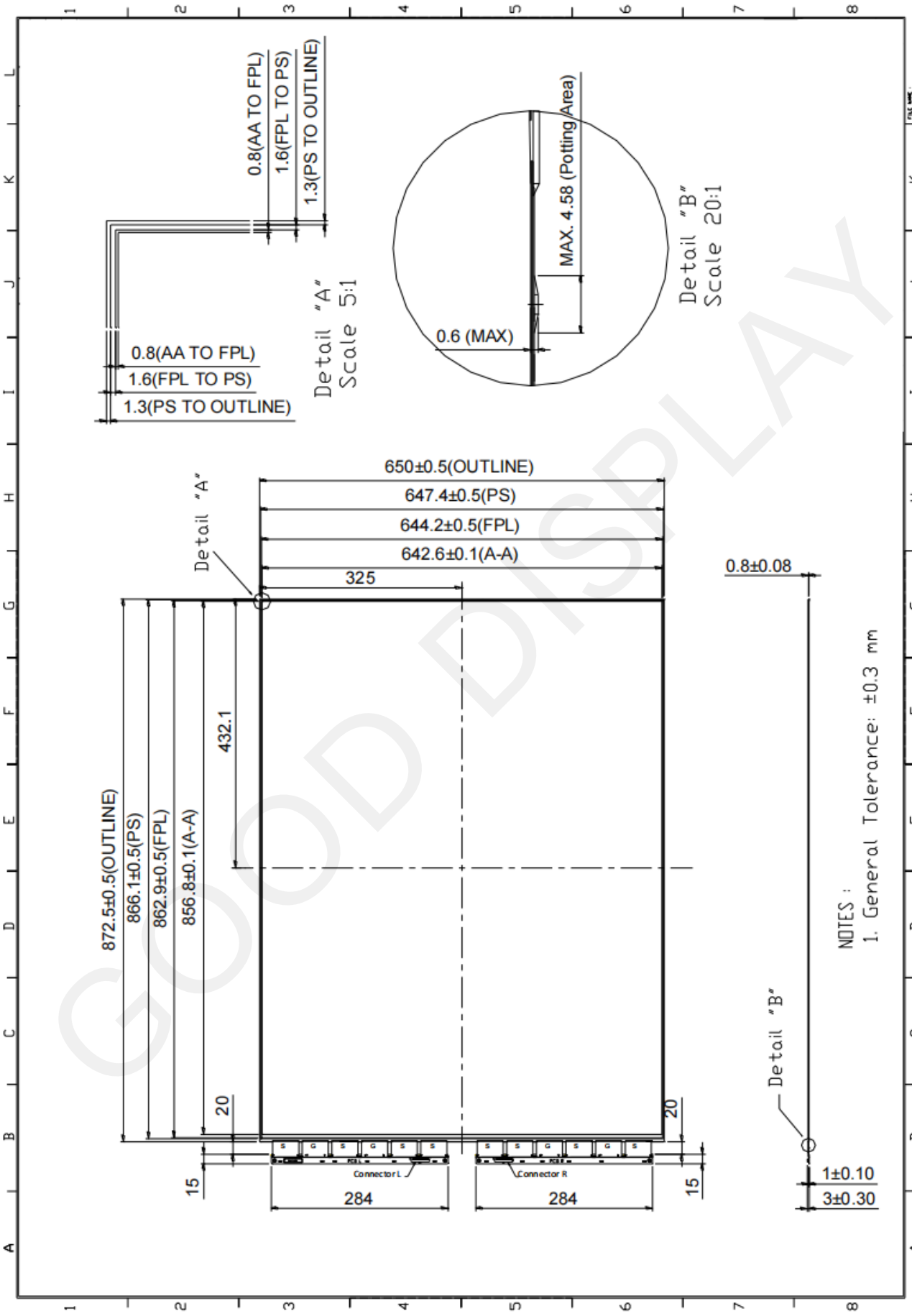
Landscape, portrait modes

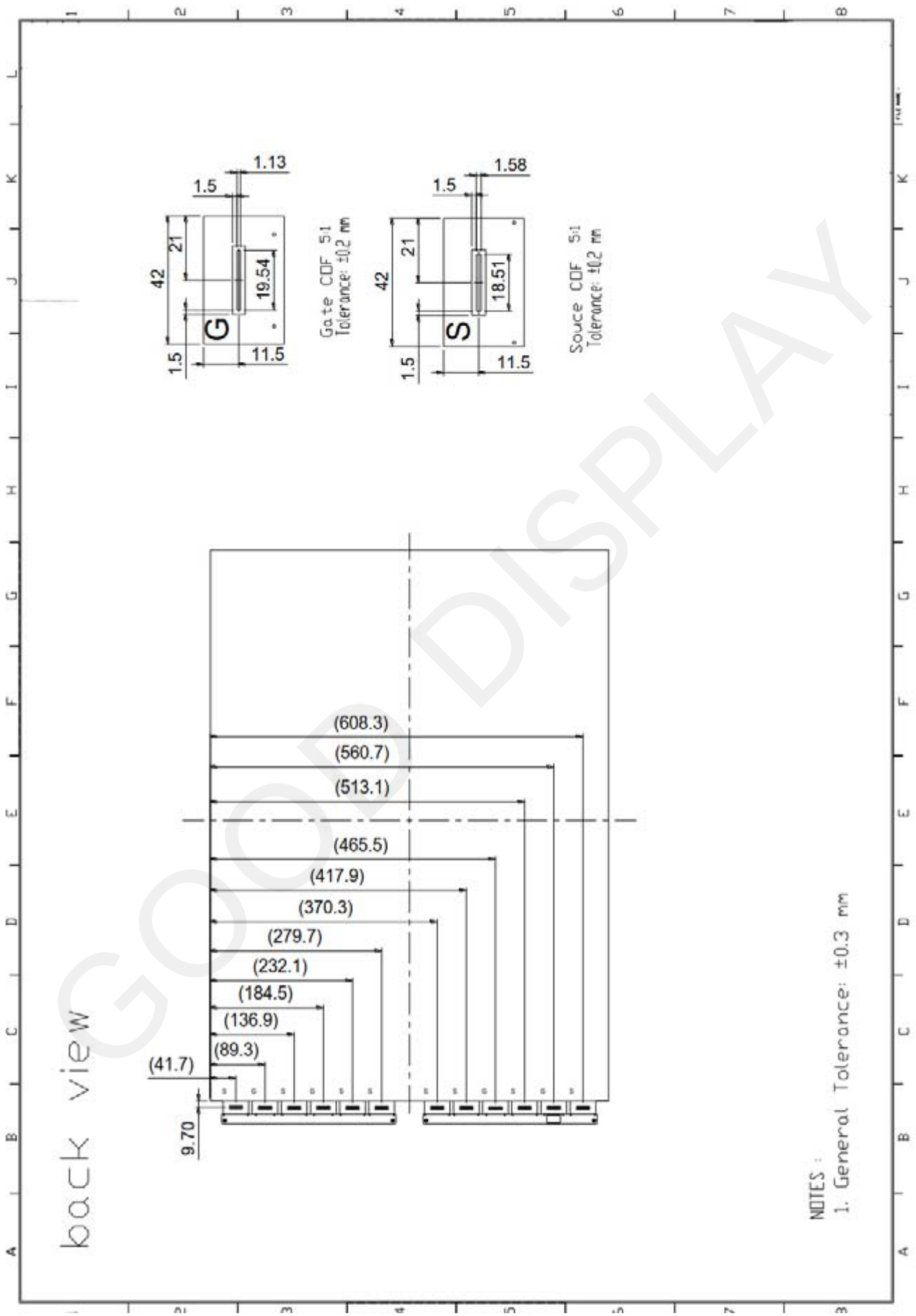
Ultra wide viewing angle

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	42"	Inch	
Display Resolution	2160 (H)×2880(V)	Pixel	3:4
Active Area	642.6(H)×856.8(V)	mm	143dpi
Pixel Pitch	0.2975	mm	
Pixel Configuration	Square		
Outline Dimension	650(H)*872.5(V)*0.805(D)	mm	
Module Weight	1100	g	
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		
Glass Substrate	0.5	mm	
Surface Treatment	Hard Coat		

4. Mechanical Drawing of EPD module





5. Input /Output Terminals

5.1 Connector type: P-TWO 196033-50041 compatible

1) **Connector L**

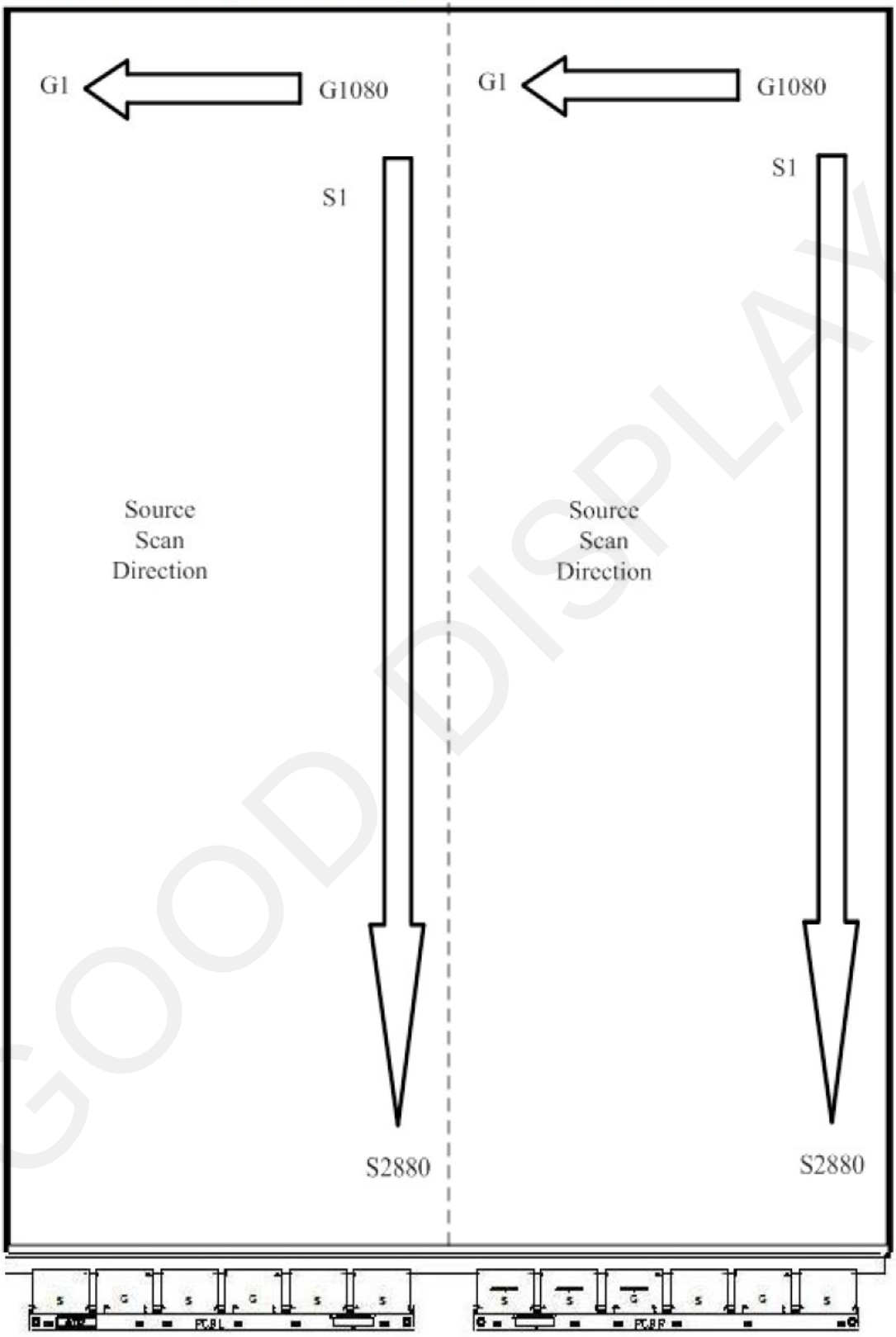
Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2_L	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_L	Output enable gate driver
7	CKV_L	Clock gate driver
8	NC	Please keep the pin floating
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_L	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	NC	Please keep the pin floating
32	XLE_L	Latch enable source driver
33	XOE_L	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VENG	Negative power supply source driver
39	VCOM_FPL	Common voltage
40	NC	Please keep the pin floating
41	SPV_L	Start pulse gate driver
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	NO Connection
46	NC	NO Connection
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	XSTL_L	Start pulse source driver

2) **Connector R**

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2_R	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1_R	Output mode selection gate driver
7	CKV_R	Clock gate driver
8	NC	Please keep the pin floating
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_R	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL_R	Start pulse source driver
32	XLE_R	Latch enable source driver
33	XOE_R	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VENG	Negative power supply source driver
39	VCOM_FPL	Common voltage
40	NC	Please keep the pin floating
41	SPV_R	Start pulse gate driver
42	NC	Please keep the pin floating
43	NC	Please keep the pin floating
44	NC	Please keep the pin floating
45	NC	NO Connection
46	NC	NO Connection
47	NC	Please keep the pin floating
48	NC	Please keep the pin floating
49	NC	Please keep the pin floating
50	NC	Please keep the pin floating

5.2 Panel Scan direction

When panel replace the image, the each sub panel need active at same time



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	V_{DD}	-0.3 to +7	V	--
Positive Supply Voltage	V_{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V	--
Max. Drive Voltage Range	$V_{POS} - V_{NEG}$	36	V	--
Supply Voltage	V_{GH}	-0.3 to +55	V	--
Supply Voltage	V_{GL}	-32 to +0.3	V	--
Supply Range	V_{GH}-V_{GL}	-0.3 to +55	V	--
Operating Temp. Range	T_{OTR}	0 to +50	℃	--
Storage Temperature	T_{STG}	-25 to +70	℃	--

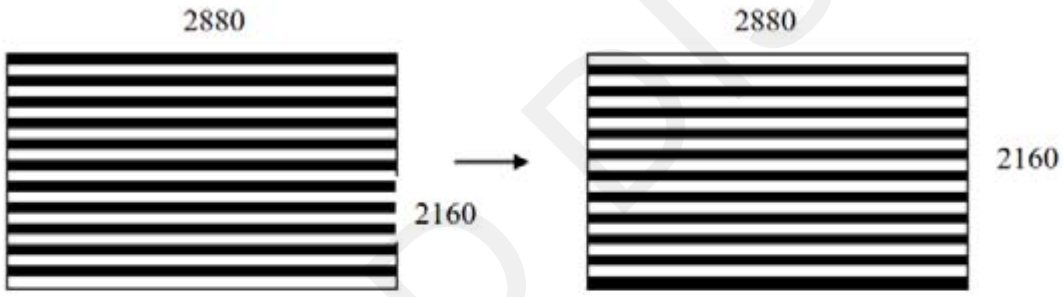
6.2 Panel DC Characteristics

this is the total current for 2 sub panel

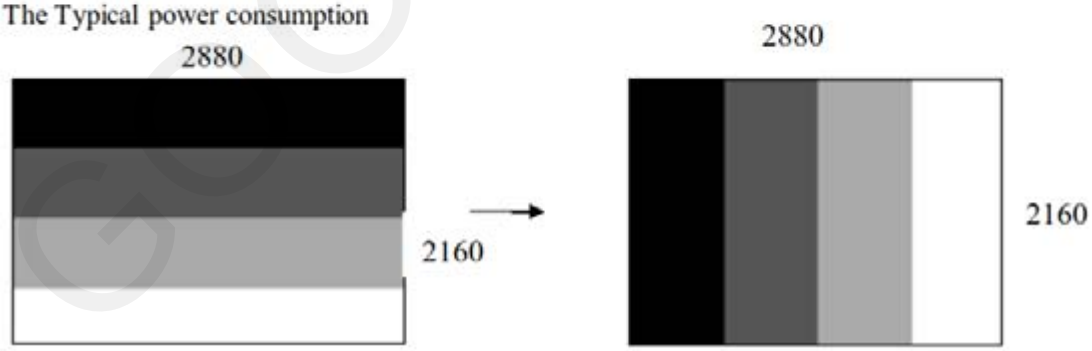
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal Ground	V_{SS}		-	0	-	V
Logic Voltage Supply	V_{DD}		2.7	3.3	3.6	V
	I_{VDD}	VDD=3.3V	-	8	13	mA
Gate Negative Supply	V_{GL}		-21	-20	-19	v
	I_{GL}	VGL = -20V		8	10	mA
Gate Positive Supply	V_{GH}		26	27	28	V
	I_{GH}	VGH = (27V)	-	8	10	mA
Source Negative Supply	V_{NEG}		-15.4	-15	-14.6	
	I_{NEG}	V_{NEG} = -15V	-	30	915	mA
Source Positive Supply	V_{POS}		14.6	15	15.4	
	I_{POS}	VPOS = 15V	-	30	915	mA
Asymmetry Source	V_{Asym}	VPOS+VNEG	-800	-	+800	mV
Common Voltage	V_{COM}		-2	Adjusted	-1	V
	I_{COM}		-	4	-	mA
Panel Power	P		-	1350	28200	mW
Standby Power Panel	P_{STBY}		-	-	1.32	mW
Rush current	IDD	VDD=3.3V	-180		180	mA
	IGL	VGL=-20V	-2750		2750	mA
	IGH	VGH=22V	-250		250	mA
	INEG	VNEG=-15V	-2850			mA
	IPOS	VPOS=15V			2850	mA
	Icom		-1900		1900	mA

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
- The Typical power consumption is measured using 50Hz waveform with following pattern transition:from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.
- Vcom is recommended to be set in the range of assigned value ± 0.1V.
- The rush current is for reference only.

Note 6-1
The maximum power consumption



Note 6-2
The Typical power consumption



6.3 Refresh Rate

The module is applied at a maximum screen refresh rate of 50Hz.

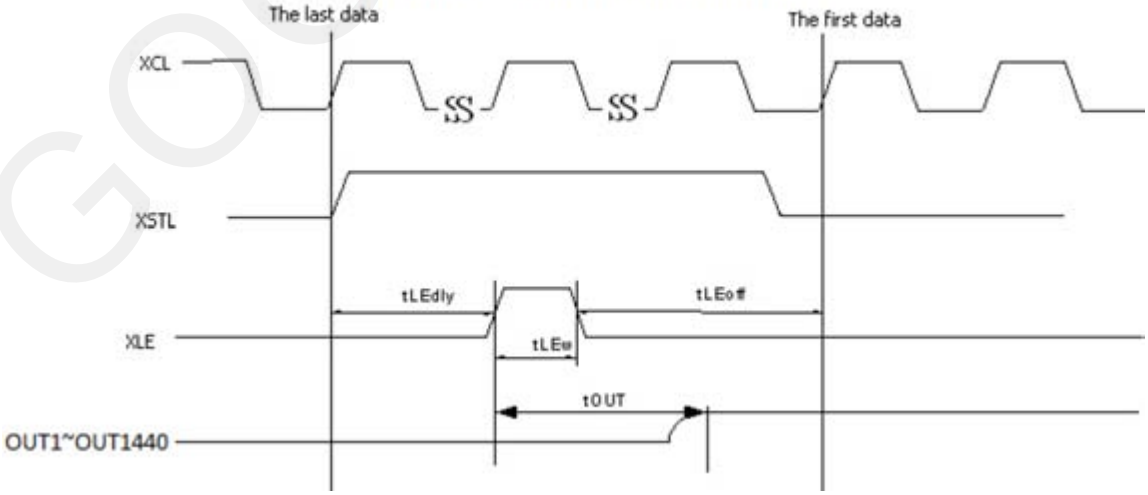
	Min	Max
Refresh Rate	-	50Hz

6.4. Panel AC characteristics

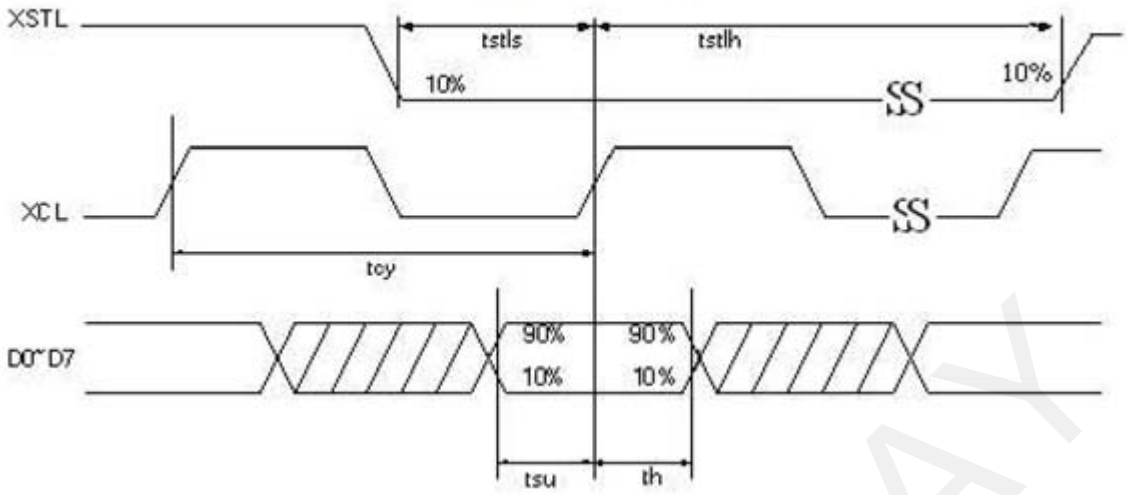
VDD=2.7V to 3.6V, unless otherwise specified.
the timing parameter for each sub panel

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum "L" clock pulse width	twL	0.5	-	-	us
Minimum "H" clock pulse width	twH	0.5			us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20	-	ns
D0 .. D15 setup time	tsu	8	-	-	ns
D0 .. D15 hold time	th	8	-	-	ns
XSTL setup time	tstls	8	-	-	ns
XSTL hold time	tstlh	8	-	-	ns
XLE on delay time	tLEdly	40	-	-	ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	12	us

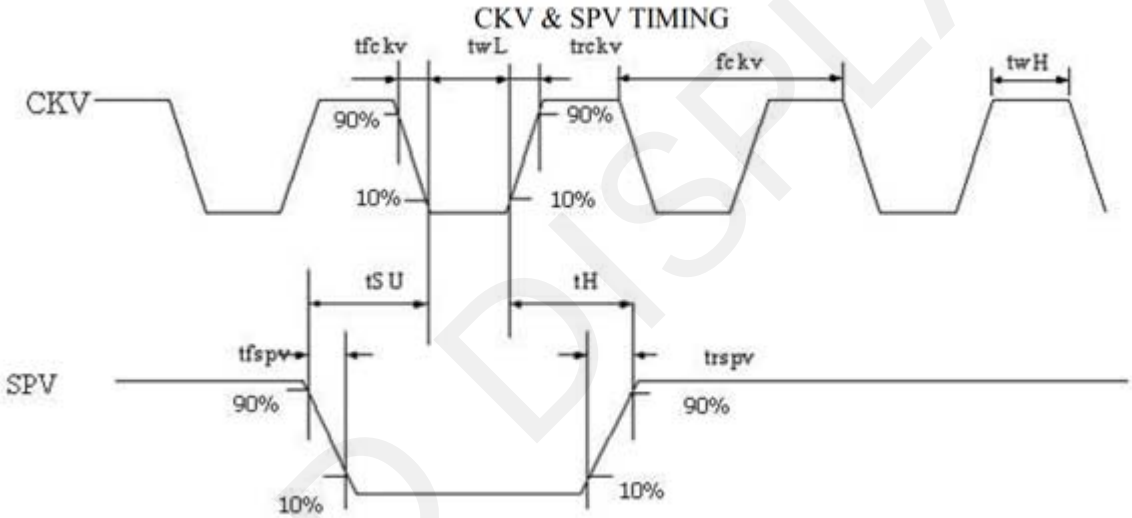
OUTPUT LATCH CONTROL SIGNALS



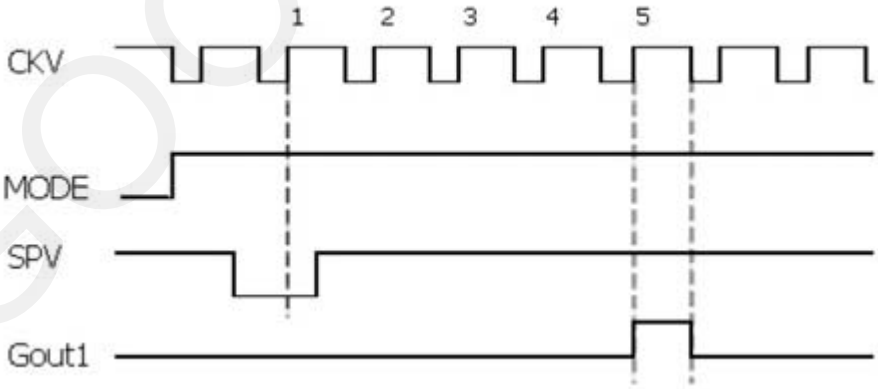
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note : First gate line on timing

After 5CLK, Gate output 1 is on.

6.5 Controllers Timing

The timing mode is depicted on Figure 6.1 and Figure 6.2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE)[3] and Gate Driver Clock (GDCK)[3]. Note, that in this mode LGON follows GDCK timing.

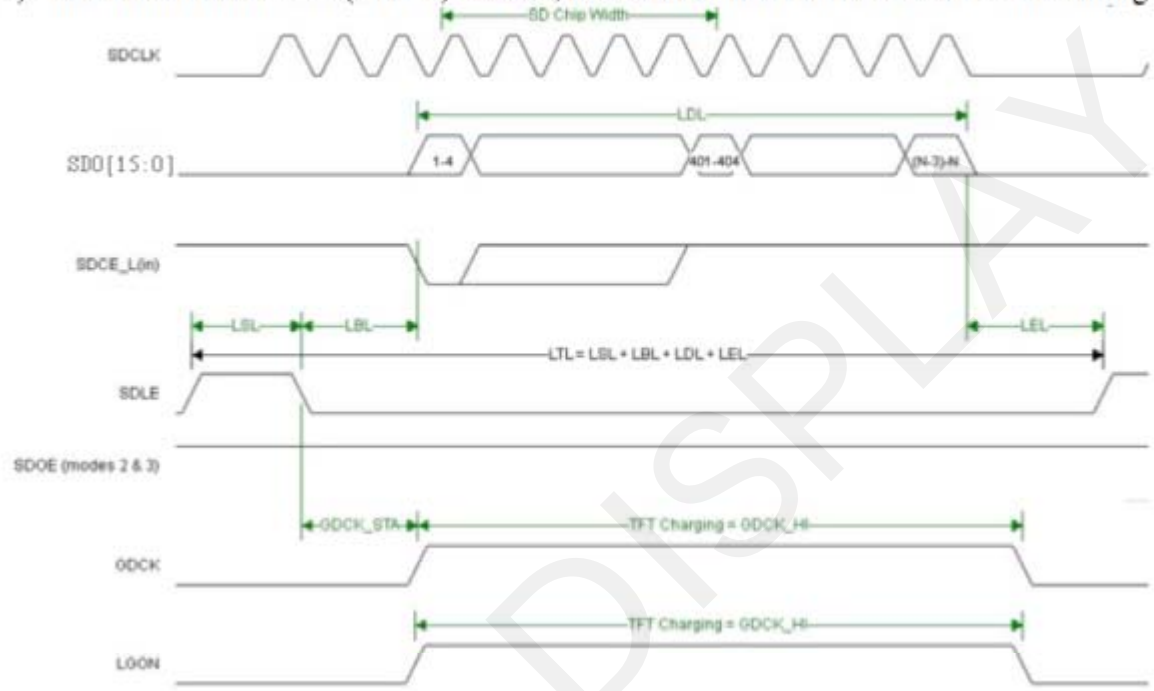


Figure 1 Line Timing in Mode 3

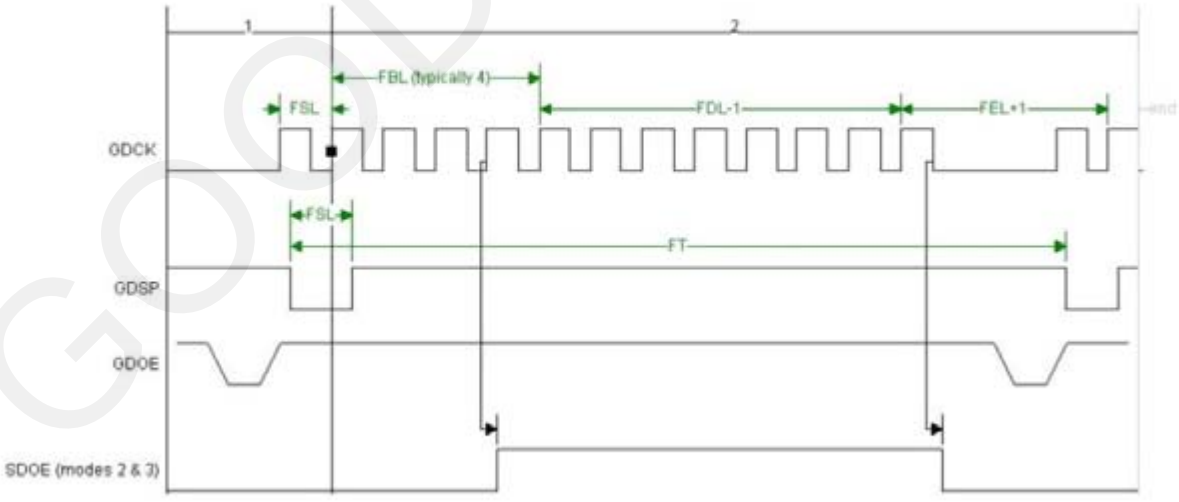


Figure 2 Frame Timing in Mode 3

Table Timing Parameters Table

For 1/2 panel

Mode	3	Resolution				2880x1080
SDCLK[MHz]	20.00					
Pixels per SDCLK	8					
Line Parameters [SDCLK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	2	4	360	1	60	204
Line Parameters [us]	-	-	-	-	-	-
	0.1	0.2	18	0.05	3.00	10.2
Frame Parameters [Lines]	FSL	FBL	FDL	FEL	-	FR[Hz]
	1	4	1,080	5	-	50.00
Frame Parameters[us]	-	-	-	-	-	-
	18.35	73.4	19818	91.75	-	-

Note 1 : For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

Note 2:

SDCLK = XCL(L /R)

SDD[15:0] = D0~D15(L/R)

SDCE_L(in) = XSTL(L /R)

GDCK = CKV(L /R)

GDSP = SPV(L /R)

GDOE = Mode1、2(L /R)

SDOE = XOE(L/R)

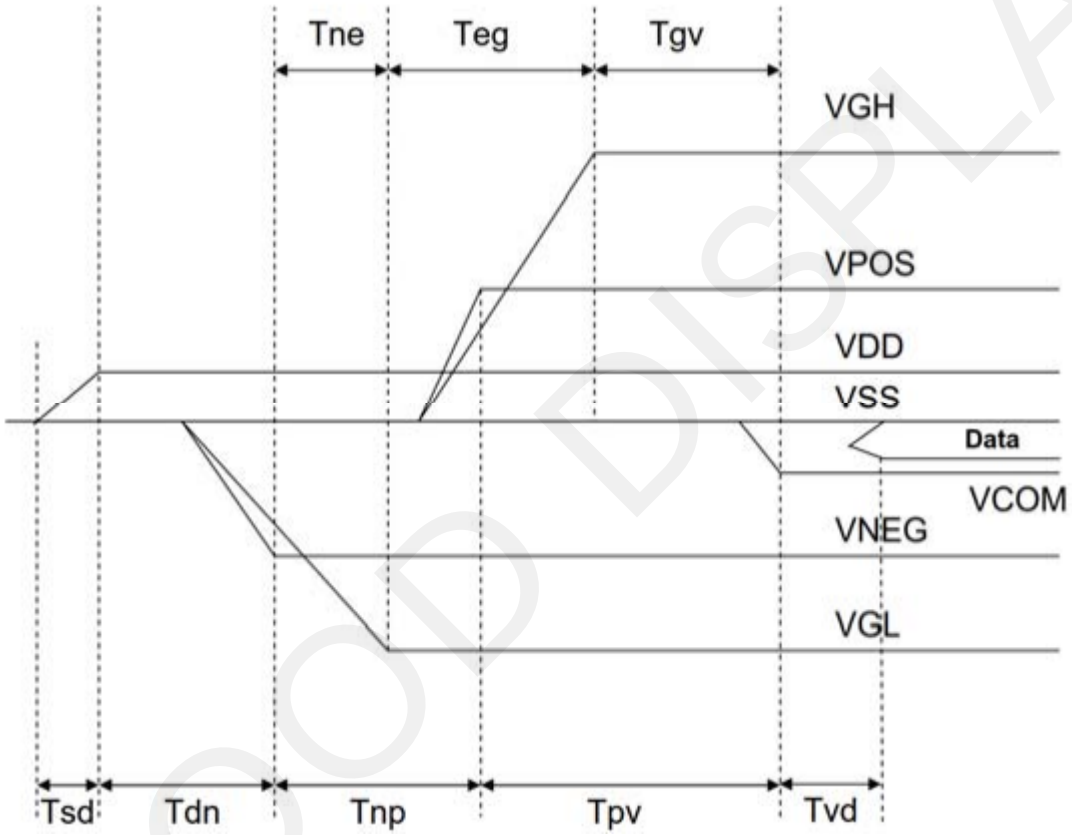
7. Power on Sequence

Power Rails must be sequenced in the following order:
1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

Note:

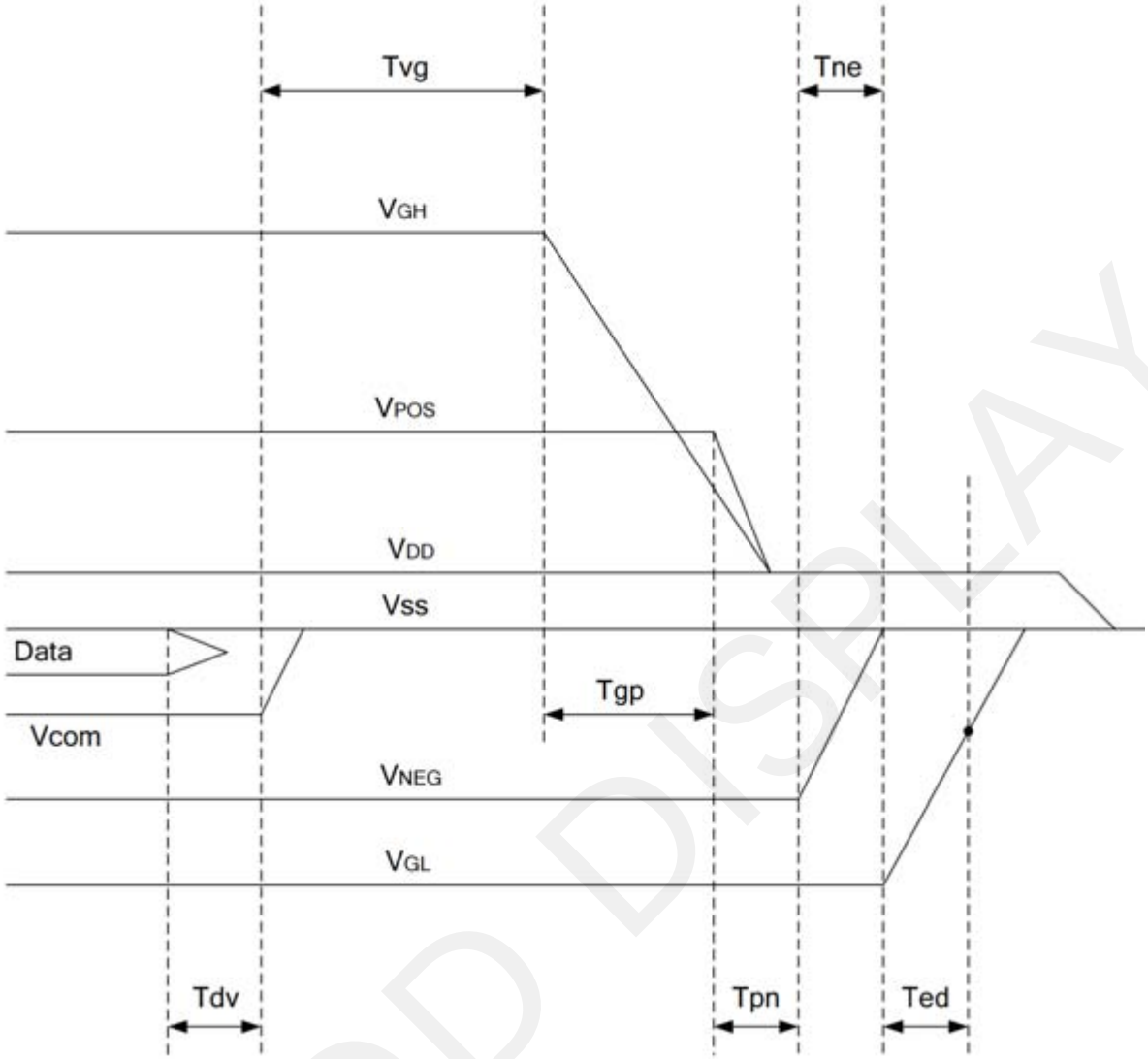
- VGL should be turned off after VNEG and VPOS have been turned off and returned to the ground state.
- VGL should be turned off after the Vcom has been turned off and returned to the ground state.
- All of Vcom/VNEG/VPOS/VGN/VGL MUST turn off right after data transfer completes.

Power on



	Min	Max
Tsd	30us	-
Tdn	100us	-
Tnp	1000us	-
Tpv	100us	-
Tvd	100us	-
Tne	0us	-
Teg	1000us	-
Tgv	100us	-

Power off



	Min	Max	
Tdv	100 μs	-	
Tvg	0 μs	-	
Tgp	0 μs	-	
Tpn	0 μs	-	
Tne	0 μs	-	
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note1：Supply voltages decay through pull-down resistors.

8. Optical Characteristics

8.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 8-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	12	-		

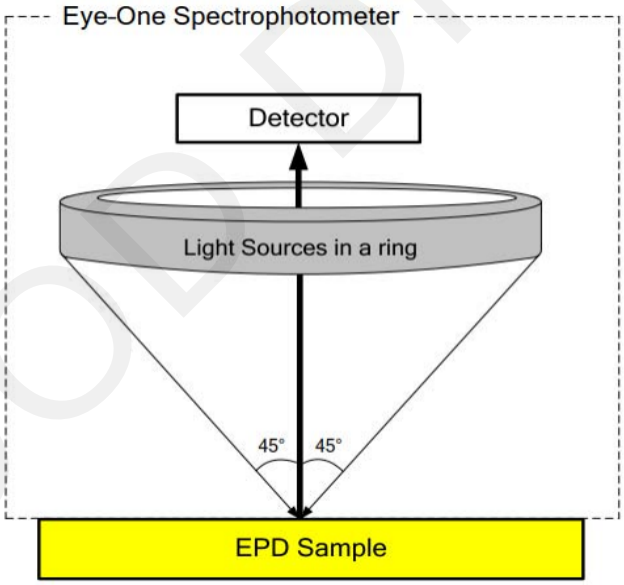
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS

m:4、8、16 when 2、3、4 bits mode

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer

8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl/Rd



8.3 Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

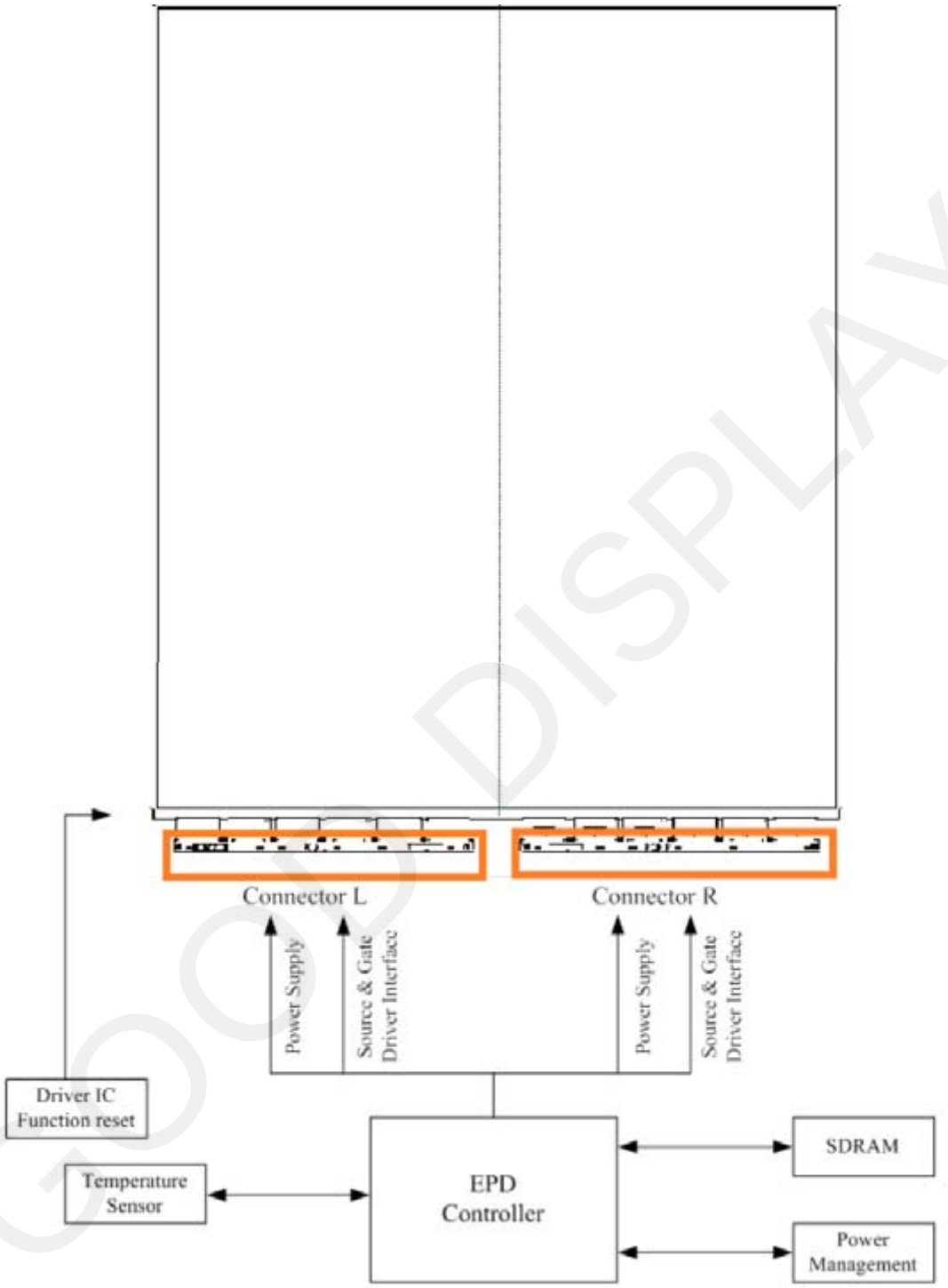
10. Reliability Test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 240 hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
8	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3 edges, 6 faces One drop for each.	Full packed for shipment	
10	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	

Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

< Criteria >
In the standard conditions, there is not display function NG issue occurred. (including: line defect ,no image). All the cosmetic specification is judged before the reliability stress.

11. Block Diagram



12. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.